

INTEGRATED CIRCUITS

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MC509, MC559/MC409, MC459

MC507, MC557/MC407, MC457

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Dual 4-Input Expander for AND-OR-INVERT Gates

Dual 4-Input Line Driver

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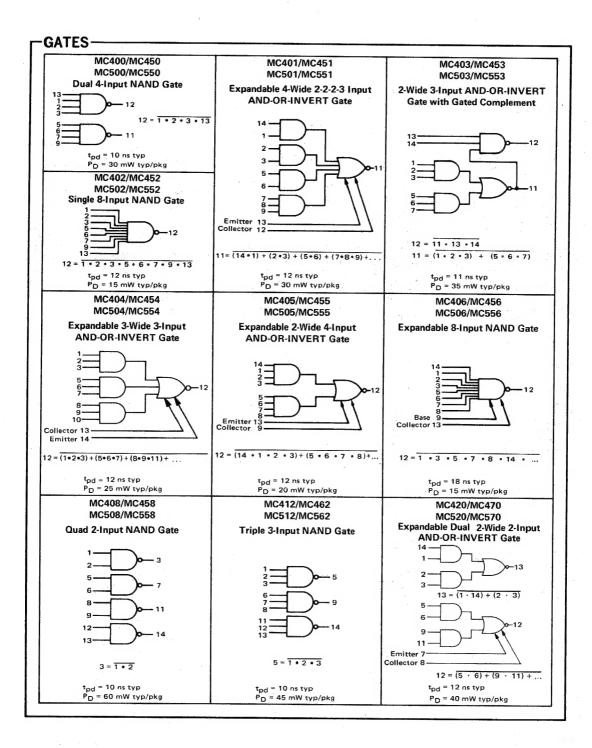
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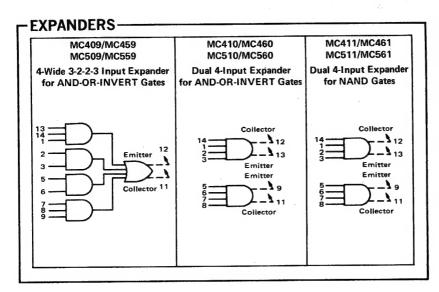
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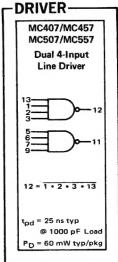
NUMERICAL INDEX (Functions and Characteristics)

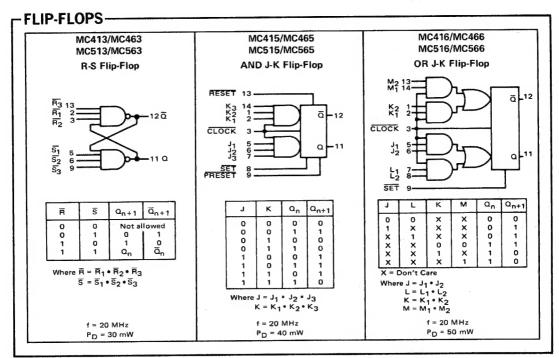
 $V_{CC} = 5.0 \text{ V, } T_A = 25^{\circ}\text{C}$

		/ре	Loa Fa	tput ding ctor Output	Propagation	Power	
Function	Case 609, 93 0 to +75°C	Case 609 55 to +125°C	MC400 Series	MC500 Series	Delay ^t pd ns typ	Dissipation mW typ/pkg	Page No.
Dual 4-Input NAND Gate	MC400 MC450	MC500 MC550	12 6	15 7	10	30	4-14
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Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC404 MC454	MC504 MC554	12 6	15 7.	12	25	4-20
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Expandable 8-Input NAND Gate	MC406 MC456	MC506 MC556	12 6	15 7	18	15	4-1:
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R-S Flip-Flop	MC413 MC463	MC513 MC563	12 6	15 7	f = 20 MHz	30	4-4
AND J-K Flip-Flop	MC415 MC465	MC515 MC565	12 6	15 7	f = 20 MHz	40	4-3
OR J-K Flip-Flop	MC416 MC466	MC516 MC566	12 6	15 7	f = 20 MHz	50	4-3
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC420 MC470	MC520 MC570	12 6	15 7	12	40	4-3











GENERAL INFORMATION SECTION

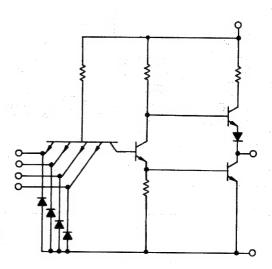
INTRODUCTION

MTTL transistor-transistor logic is a medium speed, high-noise-immunity family of saturating integrated logic circuits.

The circuits in the MTTL family are identified by a multiple emitter input transistor and an active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The active pull-up output configuration provides low impedance in the high output state. The resulting low impedances in both states provide excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 - TYPICAL MTTL CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous MC500 Series MC400 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC500 Series MC400 Series	-55 to +125 0 to +75	°c
Storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°c
Maximum Junction Temperature MC500/550 Series MC400/450 Series	+175 +150	°c
Thermal Resistance - Junction To Case $(\theta_{ m JC})$ Ceramic Flat Package Plastic Dual-In-Line	0.09 0.15	°C/m\
Thermal Resistance - Junction To Ambient (θ_{JA}) Ceramic Flat Package Plastic Dual-In-Line	0.26 0.30	°C/mV

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TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL family. Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range = 4.5 to 6.0 volts

Operating Temperature Range: MC500/550 Series = -55 to +125°C

MC400/450 Series = 0 to +75°C

Output Drive Capability

Other Gates (Output Loading Factor):

MC500 Series = 15 MC500 or MC550 Series Gates, MC550 Series = 7 MC500 or MC550 Series Gates.

MC400 Series = 12 MC400 or MC450 Series Gates.

MC450 Series = 6 MC400 or MC450 Series Gates.

Capacitance = 600 pF

Output Impedance

High State = 70 ohms (unsaturated) nominal

Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits

+5.5 volts maximum

-0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance

High State = 400 k ohms nominal Low State = 4.0 k ohms nominal

Worst-Case DC Noise Margin

High State - MC500/550 series 0.700 volt minimum MC400/450 series 0.600 volt minimum

MC500/550 series 0,750 volt minimum

MC400/450 series 0.750 volt minimum

Power Dissipation

15 mW per gate typical 40-50 mW per flip-flop typical

Switching Speeds (1)

Average Propagation Delay = 10 ns per gate typical

18 ns per flip-flop typical

Rise Time = 2.5 ns typical Fall Time = 1.5 ns typical

Flip Flop Clock Frequency (MC515/516 Series) = 20 MHz

maximum

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL gate is in the range of 107 A/s and 108 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL circuits. A comparatively large, low-inductance type capacitor (in the 1.0 µF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 µF capacitors for every eight packages throughout a breadboard is adequate to supress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL logic circuits is +5.0 Vdc.The typical average dc power dissipation is given for each MTTL circuit. (2) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.35 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL circuits.

Unused Inputs and Unused Gates

The unused inputs of any. MTTL logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical '1" level for the high state output loading is summarized for VCC = 5.0 V, V_{IL} = 0.45 V and I_{OH} = -5.0 mA:

MC500/550 Series - VOH = 2.8 volts minimum @ -55° C MC400/450 Series - VOH = 3.0 volts minimum @ 0° C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capácitance added to the expander nodes is typically 1.0 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from VCC to ground and the current that flows (approximately ISC) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC515/MC516 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition require 300 ns settling time.

require 300 ns settling time.

The direct SET, PRESET, and RESET inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct SET, PRESET, and RESET inputs do not

MTTL

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override the clock and will not control the state of the flip-flop until 120 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 20 MHz
Maximum clock fall time	= 150 ns
Minimum clock pulse width	= 20 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= -0.5 V

Note: These boundary conditions for operation are not defined as occuring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the restriction of the clock fall time. If the clock fall time is greater than 150 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 20 MHz as long as the clock fall time is less than or equal to 150 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to -0.5 volt.

(1) The switching characteristics of the MTTL family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turnon delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2}$$
 ns.

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

$$P_{D} = \frac{i_{PDL} + i_{PDH}}{2} (V_{CC})$$

where IPDL and IPDH are the typical dc current drains at VCC = +5.0 V.

MC400/450 and MC500/550 MTTL* series integrated circuits are electrically interchangeable with SUHL I[†] series logic circuits.

SG SF		-55 to	+125°C	0 to +7	5°C
NUMBERS	Description	Fan-Out = 15	Fan-Out = 7	Fan-Out = 12	Fan-Out = 6
SG40-43	Dual 4-Input NAND Gate	MC500	MC550 .	MC400	MC450
SG50-53	Expandable 2-Wide 2-2-2-3-Input AND-OR-INVERT Gate	MC501	MC551	MC401	MC451
SG60-63	Single 8-Input NAND Gate	MC502	MC552	MC402	MC452
SG90-93	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC503	MC553	MC403	MC453
SG100-103	Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC504	MC554	MC404	MC454
SG110-113	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC505	MC555	MC405	MC455
SG120-123	Expandable 8-Input NAND Gate	MC506	MC556	MC406	MC456
SG130-133	Line Driver	MC507	MC557	MC407	MC457
SG140-143	Quad 2-Input NAND Gate	MC508	MC558	MC408	MC458
SG150-153	4-Wide 3-2-2-3-Input Expander for AND-OR-INVERT Gates	MC509	MC559	MC409	MC459
SG170-173	Dual 4-Input Expander for AND-OR-INVERT Gates	MC510	MC560	MC41D	MC460
SG180-183	Dual 4-Input Expander for NAND Gates	MC511	MC561	MC411	MC461
SG190-193	Triple 3-Input NAND Gate	MC512	MC562	MC412	MC462
SF10-13	R-S Flip-Flop	MC513	MC563	MC413	MC463
SF50-53	AND J-K Flip-Flop	MC515	MC565	MC415	MC465
SF60-63	OR J-K Flip-Flop	MC516	MC566	MC416	MC466
SG70-73	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC520	MC570	MC420	MC470

^{*}Trademark of Motorola Inc. †Trademark of Sylvania Electric Products, Inc.



GENERAL INFORMATION SECTION

DEFINITIONS

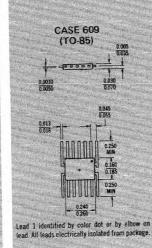
	DEFINITIONS
BVin "0"	Input breakdown voltage (ON level)
BVin "1"	Input breakdown voltage (OFF level)
CT	Total parasitic capacitance, which includes probe, wiring, and load capacitances
fTog	Toggle frequency
hee	Forward beta
IB1, IB2	Base current
IC .	Collector Current
le .	Input forward current
1in	Input current
I Company	Inverse beta current
Imax	Maximum rated power supply current with V _{max} applied
10	Output breakdown current
М	Output high current
IOL.	Output low current
IOLK	Output leakage current
IPDH	Power supply drain with inputs high
IPDL	Power supply drain with inputs low
"IR"	Input reverse current with VR applied
Isc	Short circuit current obtained from device output when one or more inputs are low
Pr	Prime fan-out
PRF	Pulse repetition frequency
PW	Pulse width
RG	Generator resistance
RL .	Load resistance
Std	Standard fan-out
tf	Fall time
toff	Turn-off delay time
ton	Turn-on delay time
^t Post	The minimal time necessary before the SET, PRESET or RESET inputs can control the flip-flop after the

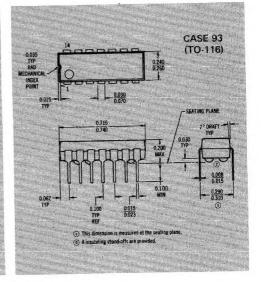
tr	Rise time
Δt _{pd}	Average increase in propagation delay per AND gate of expander when connected to an AND-OR-INVERT gate
Δt _{pd} /pF	Increased propagation delay caused by additional capacitance at expansion points
TPin	Test point at input of device under test
TPout	Test point at output of device under test
VAmp	Voltage amplitude
VBC	Base-collector voltage
VBE	Base-emitter voltage
Vc.	Collector voltage
Vcc	Power supply voltage
Vccн	High power supply voltage
VCE	Collector-emitter voltage
VCR	Collector voltage obtained thru 1.3 k ohm resistor from VCC
VCRH	Collector voltage obtained thru 1.3 k ohm resistor from VCCH
Vpc	Voltage obtained with two series diodes tied from collector to ground
V _{E1} , V _{E2} , V _{E3}	Emitter voltage
VEN	Enable voltage level
VIH	Voltage for high input voltage state
VIHX	Reduced supply voltage to hold input above thres- hold and to prevent noise from entering the device
VIL	Voltage for low input voltage state
VINH	Inhibit voltage level
V _{max}	Maximum rated power supply voltage (VCC)
Vo	Offset voltage
Voн	Output high voltage with IOH flowing out of pin
VOL	Output low voltage with IOL flowing into pin
Vout	Output voltage
Vout "0"	Output low voltage with Vth "1" applied
Vout "1"	Output high voltage with Vth "0" applied
V _R	Input reverse voltage
V _{th} "0"	Logic "0" threshold voltage
V _{th} "1"	Logic "1" threshold voltage
200	The same of the sa

PACKAGING

negative clock edge

All MTTL integrated circuits are available in the TO-85, 14-lead flat package, MC400 series is also available in the 14-lead dual in-line plastic package. To order the flat package, add suffix "F" to the basic type number; to order plastic package, add suffix "P".

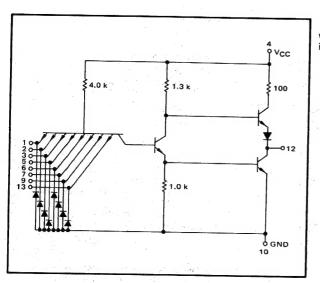




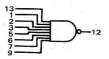
SINGLE 8-INPUT "NAND" GATE

MTTL MC500/400 series

MC502 · MC552 MC402 · MC452



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.

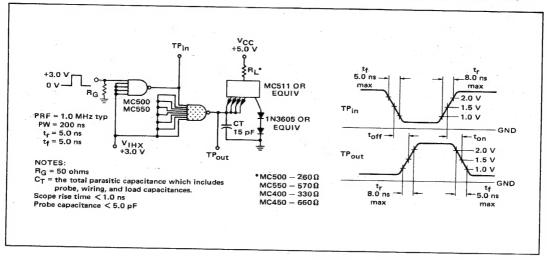


Positive Logic: 12 = 1 • 2 • 3 • 5 • 6 • 7 • 9 • 13 Negative Logic: 12 = 1 + 2 + 3 + 5 + 6 + 7 + 9 + 13

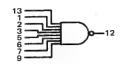
Total Power Dissipation = 15 mW typ/pkg Propagation Delay Time = 12 ns typ

SERIES					
SERIES	INPUT LOADING FACTOR	(1F)	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC502 MC552	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC402 MC452	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUITS



Test procedures are shown for only one input of the gate. To complete testing, sequence through remaining inputs in the same manner.



							TE	ST CO	NDITIC	NS						
				mA			Volts									
	@ Test	I _{OL} I _{OH} , , ,						v	., .,	V	v	v		,,		
Temperature		Pr*	Std	Pr*	Std	l'in	VIL	VIH	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}	V _{CCH}	V _{IHX}	
MC502*, MC552 {	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-	
	425°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0	
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5, 0	-	-	
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-	
MC402*, MC452	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5,0	7.0	3.0	
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-		
ACASO Tost Limite									3.4							

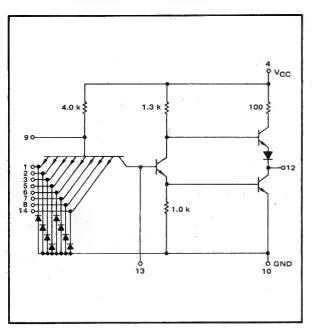
														(+75℃	20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1.	5.5	5.0	-	-	i .
	Ü	Pin		IC502,								52 Te					TEST CURI	RENT	/ VOLT	AGE	APPLIED	TO P	INS LI	STED	BELOW	/:		1
		Under		5°C		25°C	_	25°C		°C -	_	25°C	-	′5°C		<u> </u>		1.		_				1				-
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Он	lin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input				1.				100			Ť			T				Т		Γ	Γ	1	Г					
Forward Current	$I_{\mathbf{F}}$	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,5,6, 7,9,13	-	-	-	4	-	-	1,10
Leakage Current	I _R	1		100	-	100	-	100	-	100		100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Inverse Beta Current	I_{L}	1	-	100	-	100		100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-		-	4	-	-	10
Breakdown Voltage	BV _{in"0"}	1	-	-	-	5.5	-	-	-	-	-	5.5	-	-	Vdc	-	-	1	-,	-	-	-		-	4	-	-	10
	BV _{in"1"}	. 1		-	-	5.5	-	-	-	-	-	5.5	-	7 -	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Output Output Voltage	V _{out ''0''}	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-		1	-	-	4	-	-	10
	Vout "1"	12	2.5	-	2.4	-	2.7		2. 5	-	2. 4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	† -	4	-	-	10
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-		1,2,3,5,6, 7,9,10,13
Short-Circuit Current	I _{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,9,10,13
Output Voltage	V _{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	. 10
	VOH	12	2.8	-	3, 2	-	3.35	-	3.0	-	3, 1	-	3, 15		Vdc	-	12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	Imax	4	-	-	-	10	-	_	-	-	-	10	-	-	mAdc		_	-	-	-	-	-	-	-	-	4	-	1,10
Power Supply Drain	I _{PDH}	4	-	6.0	-	6.0	-	6.0	-	7. 5	-	7.5	-	7. 5	mAde	-	-	-	-	Ē	-	-	-	-	4	-		10
	I _{PDL}	4	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	mAdc	-	-	-	-	-	_	-	-	-	4	-	. 1	1,10
Switching Parameters																Pulse In	Pulse Out										. 7	
Turn-On Delay	ton	1,12	-	-	-	24	-	-	-	-	-	24	-	-	ns	1	12	-	-		-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Turn-Off Delay	toff	1,12	-	-	-	20	- `	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Rise Time	t _r	1,12		-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Fall Time	t _f	1, 12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4		2,3,5,6, 7,9,13	10

^{*}Prime Fan-Out.

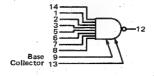
EXPANDABLE 8-INPUT "NAND" GATE

MTTL MC500/400 series

MC506 · MC556 MC406 · MC456



This device consists of an 8-input AND gate driving an output inverter. The base and the collector of the multiple emitter input transistor are available as expander terminals. The number of inputs can be expanded to 20 by using the MC511 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.

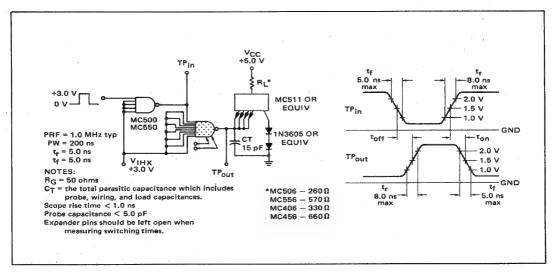


Positive Logic: 12 = 1 • 2 • 3 • 5 • 6 • 7 • 8 • 14 • Expanders Negative Logic: 12 = 1 + 2 + 3 + 5 + 6 + 7 + 8 + 14 + Expanders

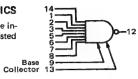
Total Power Dissipation = 15 mW typ/pkg Propagation Delay Time = 18 ns typ

SERIES	INPUT LOADING FACTOR	(I _F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC506 MC556	1	(1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC406 MC456	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0 ⁵ to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the gate. The other inputs are tested in the same manner.



		l l					116	31 CU	אוווטאי	M2						
				mA			Volts									
	@ Test	٦,	D1.	I _{OH}			v	V _{IH}	٧,	v	V _{th 0}	v	v	v	v	
Ter	mperature	Pr*	Std	Pr*	Std	'in	VIL	*н	*R	"th 1	₹th Q	Vour	*cc	V _{CCH}	VIHX	
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-	
MC506*, MC556 }	} +25℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1. 2	5.5	5.0	8.0	3.0	
	(+125℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-	
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-	
MC406*, MC456	} +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0	
MC400 , MC430	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	
140404 - 11 11																

TECT COMPLETIONS

														- 1	+/5 C	20 10	-1.2 -0.6	1.0	0, 20	3, 0	4.5	1.1	1.1	J. J	5.0	-	-	4 !
		Pin	-	MC506						AC406,							TEST CURF	RENT	/ VOLT	AGE /	APPLIED	TO PI	INS-LI	STED I	BELOW	:		
		Under		55°C		25°C		25°C		°C	_	25°C		5°C			,											
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	loı	I _{OH}	l _{in}	V _{IL}	$V_{\rm IH}$	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _F	1	-	-1. 33	-	-1. 33	-	-1. 33	-	-1.66	-	-1.66	-	-1.66	m Adc	-	-	-	-	-	2,3,5,6, 7,8,14	-	-	-	4	-	-	1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV _{in"0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-		1	-	-	-	-	-	-	4	-	-	10
	BV _{in"1"}	1	5.5	-	5. 5	-	5.5	-	5.5		5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Output Output Voltage	v _{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0. 45	-	0. 45	-	0. 45	Vdc	12	-	2	-	-	-	1	-	-	4	-	-	10
	Vout "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vde	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,8,10,14
Short-Circuit Current	ISC	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAde	~	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7, 8,10,12,14
Output Voltage	VOL	12	-	0.40		0.40	-	0:45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	- '	4	-	-	10
	VOH	12	2.8	-	3. 2	. 5	3. 35	-	3.0	- 1	3.1	-	3.15		Vdc		12	-	1	~	-	-	-	-	4	-		10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-		-	-	10		-	mAdc	-		-	-	-	-	-	-	-	-	4	-	1,10
Power Supply Drain	I _{PDH}	4	-	6.0	-	6.0	-	6.0	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-		-	-	-	4	-	-	10
	I _{PDL}	4	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0		3.0	mAdc	-	-	-	-	-	-	-	-		4	-	-	1,10
Switching Parameters Turn-On Delay	, ton†	1, 12	-	-	-	28	-	-	_	-	-	.28	-		ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	4		2,3,5,6 7,8,14	, 10
Turn-Off Delay	toff	1,12	-	-	-	20	-	-		-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6 7,8,14	10
Rise Time	t _r	1,12	-	-	-	8.0	-	-	-		-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6 7,8,14	, 10
Fall Time	t _f	1,12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12		-	-	-	-	-	-	4	-	2,3,5,6 7,8,14	, 10

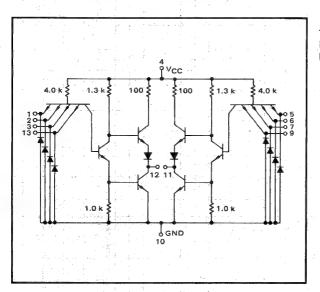
^{*} Prime Fan-Out.

[†] Add 3.0 ns for each AND expander (1/2 MC511, MC561, MC411, and MC461) used. Add 2.0 ns tod for each pF added to either expander points.

DUAL 4-INPUT "NAND" GATE

MTTL MC500/400 series

MC500 · MC550 MC400 · MC450



This device consists of two 4-input NAND gates. The gates can be cross-coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.

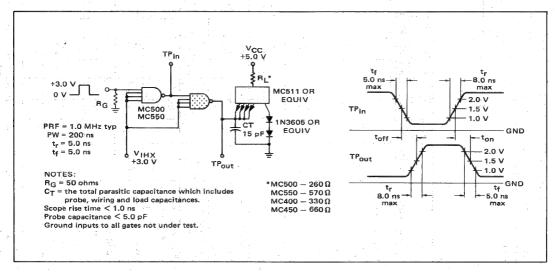


Positive Logic: 12 = 1 • 2 • 3 • 13 Negative Logic: 12 = 1 + 2 + 3 + 13

Total Power Dissipation = 30 mW typ/pkg Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR (IF)	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC500 MC550	1 (-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC400 MC450	1 (-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to:+75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



			-				TE	ST CO	NDITIO	NS					
				mA							Volts				
	@ Test	I,	DL	ار	Н		v	v	v	v	v	v	v	v	v
Te	nperature	Pr*	Std	Pr*	Std	'in	Λ ^{IΓ}	V _{IH}	V _R	V _{th 1}	Vibo	Vout	Vcc	V _{ссн}	ViHX
	_55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5:0	-	-
MC500*, MC550	} +25℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
MC400*, MC450	₹ +25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
•	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

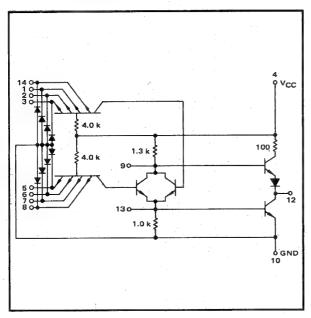
								-						,	+/3 C	20 10	-1.2 -0.0	1.0	0.40	1 3.0	4.0	1.7	1.1	0.0	5.0		-	
		Pin		AC500								50 Te					TEST CURI	RENT	/ VOLT	AGE /	APPLIED	TO P	INS LI	STED	BELOW	1:		1
		Under	_	55°C	_	25°C		25°C)°C		25°C		′5°C			1 .							,			г	-
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Іон	in	VIL	VIH	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{CCH}	V _{IHX}	Gnd †
Input			-	Π		Г		Г				Ι							Γ]					
Forward Current	I _F	1	-	-1.33	-	-1.33		-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,13	- "	-	- '	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,13
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	7-	-	. 1	-	1-1	-	4	-	-	10
Breakdown Voltage	BV _{in''0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5		5.5	-	Vdc	-	-	1	-	-	, -	-	-	-	4	-	-	10
	BV _{in"1"}	- 1	5.5	-	5.5	-	5.5	-	5,5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,13
Output Output Voltage	V _{out ''0''}	12	-	0.45		0.45	-	0.45	_	0.45	-	0.45		0. 45	Vdc	12	_	-	_	_	_	1	_	_	4		_	10
	v _{out "1"}	12	2. 5		2.4	-	2.7	-	2. 5	-	2.4	1-	2.5	-	Vdc		12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I _{OLK}	12	-	250	-	250		250	-	250	-	250	-	250	μAde	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3, 10,13
Short-Circuit Current	ISC	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-		1,2,3, 10, 12, 13
Output Voltage	V _{OL}	12		0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	- ,	10
	V _{OH}	12	2.8	-	3. 2	-	3.35	-	3.0	-	3. 1	-	3. 15	-	Vdc	-	12	-	- 1	-	-	-	-		4	-	1,-	10
Power Requirements (Total Device) Maximum Power Supply Current	Imax	4 ;	-			10		-	-	-	-	10	-	-	mAde	-		-	-	-	-	_	-	-	-	- 4	-	1,5,10
Power Supply Drain	I _{PDH}	4	-	12		12	-	12	-	15	-	15	-	15	mAde	_	 	<u> </u>		- -		-	 _	-	4		-	101
	I _{PDL}	4	-	6.0		6.0	-	6.0	-	6.0	-	6.0	-	6.0	mAdc	-	-	-	-	-	-	-	-	-	4	-		1,5,10
Switching Parameters	FDE		-		1	-	-	-	\vdash	<u> </u>	+			\vdash		Pulse In	Pulse Out	\vdash		_			-	 				
Turn-On Delay	ton	1,12	-	-	<u> </u> -	20	<u> </u>	-	<u> </u>	-	- "	20	-	-	ns	1	12	-	-	-	-		-	-	4	y =	2,3,13	
Turn-Off Delay	toff	1,12	-		-	20	-		<u> </u>	-	_	20	-	-	ns.	1	12	-	-	-	-		-	-	4	÷	2,3,13	
Rise Time	tr	1,12	-	-	-	8.0	-	-	-	-	. 3	8.0	-	<u> </u>	ns	1	12	-		-	-		-	-	4	5 -	2,3,13	
Fall Time	t _f	1,12	-	-	-	5.0	- 1	-	-	- :		5.0	-	-	ns	1	12	- :	-	-	-	-	-	1 -	4	[-]	2,3,13	10

[†] Ground inputs to gates not under test during ALL tests, unless otherwise noted. ‡ The inputs of all gates must be ungrounded.

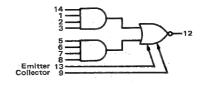
EXPANDABLE 2-WIDE 4-INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC505 · MC555 MC405 · MC455



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 or MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds

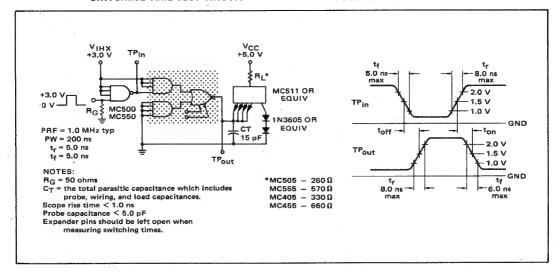


Positive Logic: 12 = (1 • 2 • 3 • 14) + (5 • 6 • 7 • 8) + (Expanders) Negative Logic: 12 = (1 + 2 + 3 + 14) • (5 + 6 + 7 + 8) • (Expanders)

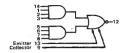
Total Power Dissipation = 20 mW typ/pkg Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC505 MC555	1	(~1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC400 MC450	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0 [®] to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.



TEST CONDITIONS mÅ Volts @ Test V_{th 1} V_{th 0} Vcc V_{CCH} Temperature Pr* Std Pr* Std ~55°C 20 10 -1.5 -0.7 1.0 0.45 2.8 4.5 2.0 1.0 5.5 5.0 MC505*, MC555 +25°C 20 10 -1.5 -0.7 1.0 0.45 2.8 4.5 1.7 1.2 5.5 5.0 8.0 3.0 (+125℃ 20 10 -1.5 1.4 0.9 5.5 5.0 -0.7 1.0 0.45 2.8 4.5 0°C 20 10 -1.2 -0.6 1.0 0.45 3.0 4.5 1.9 1.1 5.5 MC405*, MC455 -1.2 -0.6 1.0 0.45 3.0 20 10 4.5 3.0

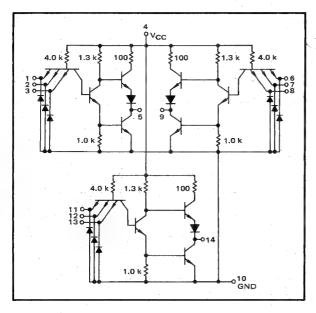
														(+75°C	20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-	
		Pin		VIC505						NC405			-				TEST CUR	RENT	/ VOLT	AGE /	APPLIED	TO P	INS LI	STED	BELOW	/:		
Characterists.	Cll	Under		55°C	_	25°C		25°C		0°C		25°C		′5°C	l		т.									,	V	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	OF	I _{ОН}	^J in	V _{IL}	VIH	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input	1.	Γ		1							Γ				1	<u> </u>	Τ	_	T	l				1.1				I
Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66		-1. 66	mAdc	_	-	_	-	_	2,3,14	-	-	-	4	-	-	1,5,6,7, 8,10
Leakage Current	I_{R}	1	-	100		100	-	100	-	100	-	100	-	100	μAde	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Inverse Beta Current	I _L	1 .	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	5,6,7,8,10
Breakdown Voltage	BV _{in "0"}	1	5,5	-	5.5	-	5.5	-	5.5	-	5.5	- '	5.5	-	Vdc	-	-	1	-	-	-		-	-	4	-	-	5,6,7,8,10
	BV _{in "1"}	1	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-		1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Output																												
Output Voltage	V _{out ''0''}	12	-	0, 45	-	0.45	-	0.45		0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-		1	-	<u> </u>	4	-	-	5,6,7,8,10
	vout "1"	12	2.5	-	2.4		2.7	-	2.5	-	2,4	-	2.5	-	Vdc	-	12	-	-		-	-	1	_	4	7	-	5,6,7,8,10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,8,10,14
Short-Circuit Current	ISC	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,10, 12,14
Output Voltage	V _{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	'4	-	-	5,6,7,8,10
	V _{ОН}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	5,6,7,8,10
Power Requirements									$\overline{}$																			
(Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6, 7,8,10,14
Power Supply Drain	I _{PDH}	4	-	7.0		7.0	-	7.0	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I _{PDL}	4	-	4.0	~	4.0	-	4.0	-	4.0	-	4.0	-	4.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,10,14
Switching Parameters																Pulse in	Pulse Out											
Turn-On Delay	t _{on}	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Turn-Off Delay	toff	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	- 1	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Rise Time	tr	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Fall Time	t _f	1,12	-	-	-	6.0	-	-	-	-	-	6.0	-	-	ns	, 1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10

^{*} Prime Fan-Out

MTTL MC500/400 series

TRIPLE 3-INPUT "NAND" GATE

MC512 · MC562 MC412 · MC462



This device consists of a 3-input AND gate driving an output inverter. This gate can be used to build a pulse shaping network for interfacing with discrete component circuits.

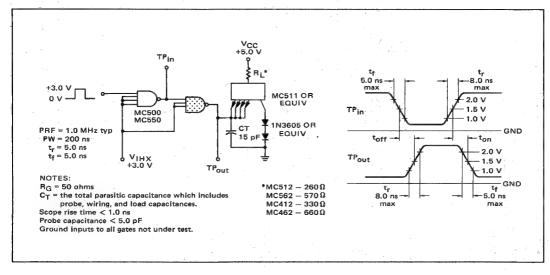


Positive Logic: $5 = 1 \cdot 2 \cdot 3$ Negative Logic: 5 = 1 + 2 + 3

Total Power Dissipation = 45 mW typ/pkg Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(iF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC512 MC562	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC412 MC462	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	4						TE	ST CO	NDITIO	NS					
				mA							Volts				
	@ Test	ار	DL	Ic	Н		v	v	v	V _{th 3}	V	Vout	٧ _{cc}	v	v
Ten	nperature	Pr*	Std	Pr*	Std	in	V _{IL}	VIH	V _R	Tth 1	V _{th 0}	out	*cc	V _{CCH}	VIHX
1994	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0		-
MC512*, MC562	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	4	
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	_
MC412*, MC462	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	- 1	-

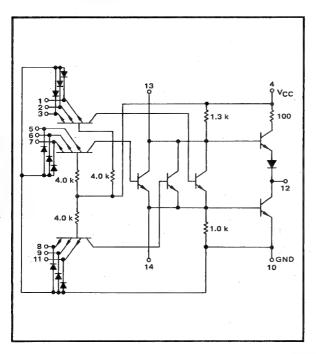
															+/3 €	20 10	-1.2 -0.0	1.0	0, 40	3.0	4.5	1.7	1 4 4	10.0	0.0		L	1
		Pin	_	MC512	•					1C412,							TEST CURI	RENT	/ VOLT	AGE A	PPLIED	TO P	INS L	ISTED I	BELOW	<i>l</i> :		
Characteristic	Symbol	Under Test	Min	55°C Max	_	25°C Max	-	25°C Max		°C Max		25°C Max		5°C Max	Unit	loL	I _{OH}	Iin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th O}	V _{out}	V _{cc}	V _{CCH}	V _{IHX}	Gnd †
Input Forward Current	I _F	1	-	-1.33	1	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	r	-	-	_	-	2,3		-	-	4	-		1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-		-	-	-	1	-	-		4	-	-	10
Breakdown Voltage	BV _{in''0''}	1	5.5	-	5. 5	-	5.5	-	5. 5		5, 5	-	5.5		Vdc	4	-	1	-	-		-	-		4	-		10
	BV _{in"1"}	1	5.5	- '	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-		1	-	-	- ,	-	-	- 1	4	-	•	2,3,10
Output Output Voltage	v _{out "0"}	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	_	-	-	-	-	1	-	-	4	-	-	10
	V _{out ''1''}	5	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	5	-	-	-		-	1	-	4	-	-	10
Leakage Current	IOLK	5	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	5	4	-	•	1,2,3,10
Short-Circuit Current	I _{SC}	5	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	, : <u>-</u>	1,2,3, 5,10
Output Voltage	V _{OL}	5	-	0.40	-	0.40		0.45	-	0.40	-	0.40	-	0.45	Vdc	5	-	- 1	-	1			-	-	4	-	1.2	10
	V _{OH}	5	2.8	-	3.2	-	3.35	-	3.0	-	3.1		3.15	-	Vdc	-	5	-	1	-	-	-	-	-	4	~	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-		15	-	_	-	-		15		_	mAdc	-	_	-	-	-	-	-	-	-		4	-	1,6,10,11
Power Supply Drain	IPDH	4	-:	18	-	18		18	-	22.5	-	22.5	-	22.5	mAdc	-	-	-	-	-	-	-	-		4	1	-	10 ‡
	I _{PDL}	4	-	9.0	-	9, 0	-	9.0	-	9:0	-	9.0	-	9.0	mAdc	-		-	-	-	7		_	-	4	-	1	1,6,10,11
Switching Parameters Turn-On Delay	ton	1,5	_	_	_	20	_ :	_	-	-	_	20	-	_	ns	Pulse In	Pulse Out	-	_	-	-	-	-	-	4		2,3	10
Turn-Off Delay	toff	1,5	 -	-	-	20	-	-	-	-	-	20	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Rise Time	tr	1,5	-	-	-	8.0		-	-	_		8.0	Ξ		ns	1	5		-	. =	-	-	-	-	4	-	2,3	10
Fall Time	t.	1,5	-	-	-	5.0	-	-	_	-	-	5.0	-	-	ns	1	5	-	-	-	-	-	-	T -	. 4	-	2,3	10

^{*} Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

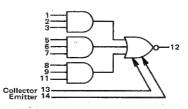
EXPANDABLE 3-WIDE 3-INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC504 · MC554 MC404 · MC454



This device consists of three 3-input AND gates ORed together driving an output inverter. The common ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC500 or the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



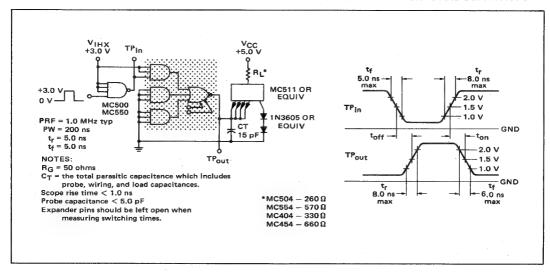
Positive Logic: 12 = (1 • 2 • 3) + (5 • 6 • 7) + (8 • 9 • 11) + (Expanders) Negative Logic:

12 = (1 + 2 + 3) • (5 + 6 + 7) • (8 + 9 + 11) • (Expanders)

Total Power Dissipation = 25 mW typ/pkg Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I _F)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC504 MC554	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC404 MC454	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



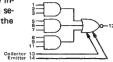
5,6,7,8,9,

10,11

2,3

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.



6.0

1,12

							- 11	:ST CU	טוזזטאיי	CPI					
				mA							Volts				
	@ Test	I,	DL	I,	ЭН		v	v	v	v	v	v	V _{cc}	v	VIHX
To	emperature	Pr*	Std	Pr*	Std	'in	A ^{IF}	V _{IH}	V _R	V _{th 1}	*th 0	Vout	*cc	V _{ссн}	*IHX
	(-55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
IC504*, MC554	₹ +25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	20	10	-1.2	-0.6	1.0	0,45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
IC404*, MC454	} +25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

MC504, MC554 Test Limits MC404, MC454 Test Limits Pin TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: +25°C +125°C +25°C +75°C Under −55°C VIHX V_{cc} V_{CCH} Min Max Min Max Min Max Min Max Min Max Min Max Unit loL Gnd Characteristic Symbol Test input 1.5.6.7.8 -1.33 -1.33 -1.33 -1.66 -1,66 -1.66 mAde 2,3 Forward Current 9,10,11 2,3,5,6,7 100 100 100 100 100 100 Leakage Current 1 8,9,10,11 5,6,7,8,9 100 100 µ Ado Inverse Beta Current 100 100 100 100 10,11 5,6,7,8,9 5.5 5.5 Vdc Breakdown Voltage 5.5 BV in "0" 10.11 5.5 5.5 Vdc 1 2.3.5.6.7 BV ... "1" 5.5 5.5 5.5 5.5 1 8,9,10,11 Output 1 5,6,7,8,9 0.45 0.45 0.45 0.45 12 12 0.45 0.45 Output Voltage Vout ''0' 10,11 5,6,7,8,9 12 2.7 2.5 2.4 2.5 Vdc 12 V_{out ''1''} 10,11 12 1,2,3,5,6 4 250 250 250 250 250 250 μAde Leakage Current 12 IOLK 7,8,9, 10,11 1,2,3,5,6, -45 -10 -45 -10 -45 -10 -45 mAde 4 Short-Circuit -10 -45 -10 -45 -10 7,8,9,10, Current 11,12 5,6,7,8,9, 4 Output Voltage 12 0.40 0.45 0.40 0.40 - 0.45 12 v_{ol} 10.11 5,6,7,8,9, 12 12 2.8 1 VOH 3.2 3.35 3.0 3.1 3.15 10.11 Power Requirements (Total Device) Maximum Power 10 1.2.3.5.6. 10 mAdc 4 Imax 7,8,9, 10,11 Supply Current 10 10 10 10 mAdc 4 -Power Supply Drain 4 8.0 8.0 8.0 I_{PDH} 1,2,3,5,6, 4 6.0 6.0 6.0 6.0 6.0 6.0 mAdc I_{PDL} 7,8,9, 10,11 Pulse In Pulse Out Switching Parameters 5,6,7,8,9 4 2,3 22 22 Turn-On Delay 1,12 ns 10,11 4 2,3 5,6,7,8,9, 22 1 12 1,12 22 Turn-Off Delay toff 10,11 5.6,7,8,9, 8.0 1 12 4 2,3 Rise Time 1,12 8.0 t_r 10,11

6.0

1

12

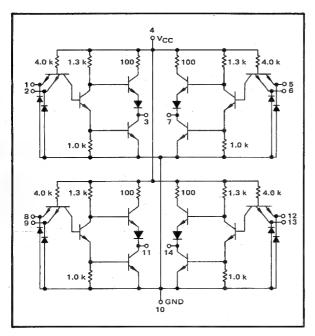
Fall Time

^{*} Prime Fan-Out

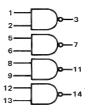
MTTL MC500/400 series

QUAD 2-INPUT "NAND" GATE

MC508 · MC558 MC408 · MC458



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flipflop may be obtained if each pair of gates is externally cross-coupled.

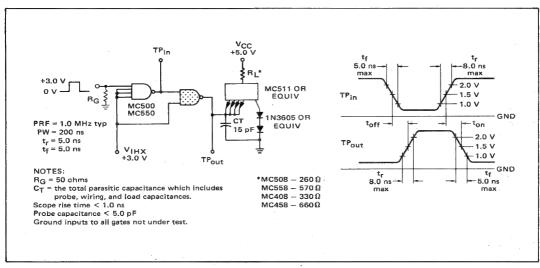


Positive Logic: $3 = 1 \cdot 2$ Negative Logic: 3 = 1 + 2

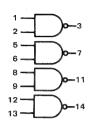
Total Power Dissipation = 60 mW typ/pkg Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(I _F)		OUTPUT DRIVE	(1 ₀ L)	TEMPERATURE RANGE
MC508 MC558	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC408 MC458	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



							TE	ST CO	NDITIO	NS					
				mA							Volts				
	@ Test	l _e	DL .	ار	Н		V _{IL}	V _{IH}	V _R	v	v	Vout	٧ _{cc}	v	v
Ŧ	emperature	Pr*	Std	Pr*	Std	1in	, IL	* IH	*R	V th 1	V _{th O}	out	*cc	V _{CCH}	V _{IHX}
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
C508*, MC558	} +25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5, 0		-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
C408*, MC458	{ +25℃	20	10	-1. 2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-
459 Toct Limi	e l														

		Pin				558 Te				C408,						,	TEST CUR	RENT	/ VOLT	AGE /	APPLIED	TO P	INS LI	STED	BELOW	l:]
Characteristic	Symbol	Under Test		55°C Max		25°C Max		25°C Max		°C Max		25°C Max		75°C Max	Unit	lor	l _{OH}	l _{in}	VIL	V _{IH}	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd†
Input Forward Current	1	1		-1. 33	<u> </u>	-1. 33	<u> </u>	-1. 33	_	-1, 66	Ī.	-1.66	-	-1.66	mAde	_		_	Ī .	_	2	Ι.			4			1,10
Leakage Current	I _F	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,10
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	_	10
Breakdown Voltage	BV _{in"0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	=	-	-	-	4	-	-	10
	BV _{in"1"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	_	Vdc	-	-	1	-			-	-	-	4	-	-	2,10
Output Output Voltage	v _{out ''0''}	3	-	0.45	-	0.45	-	0.45	_	0.45	-	0. 45	-	0.45	Vdc	3	-	-	-	-	-	1	-	-	·4	-	-	10
	Vout "1"	3	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2. 5	-	Vdc	-	3	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I _{OLK}	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	3	4	-	-	1,2,10
Short-Circuit Current	ISC	3	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10
Output Voltage	v _{OL}	3	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	-	-	-	1	-	-	-	-	4	-	-	10
	V _{ОН}	3	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3. 15	-	Vdc	-	3	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,5,8,10,12
Power Supply Drain	I _{PDH}	4	-	24	-	24	-	24	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I _{PDL}	4	-	12	-	12	-	12	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,5,8,10,12
Switching Parameters Turn-On Delay	t	1,3	_	_	_	20	_	_		_	_	20	_	_	ns	Pulse In	Pulse Out	_	_	_	_	_	_	_	4	-	2	10
Turn-Off Delay	t off	1,3	-		-	20	-	-	-	-	-	20		 -	ns	1	3	-	-	-	-	-	-		4	-	2	10
Rise Time	t	1,3	-	-	-	8.0	-	-	-		-	8.0	-	 - -	ns	1	3	-	-	-	-	-	-	-	4		2	10
Fall Time	t _f	1,3	-	-	-	5.0	-	/5 = ·	-	-	-	5.0	-	-	ns	1.	3	-	-	-	-	-	-	-	4	-	2	10

^{*} Prime Fan-Out.

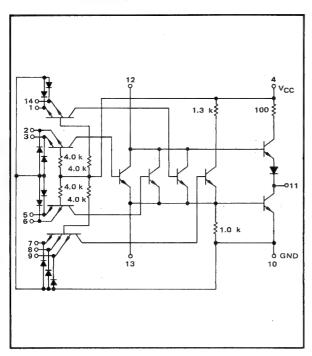
[†] Ground inputs to gates not under test, during ALL tests unless otherwise noted.

The inputs to all gates must be ungrounded.

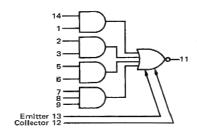
EXPANDABLE 4-WIDE 2-2-2-3 INPUT "AND-OR-INVERT" GATE

MTTL MC500/400 series

MC501 · MC551 MC401 · MC451



This device consists of three 2-input and one 3-input AND gates internally ORed together and then inverted to provide the output. The common ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 and the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

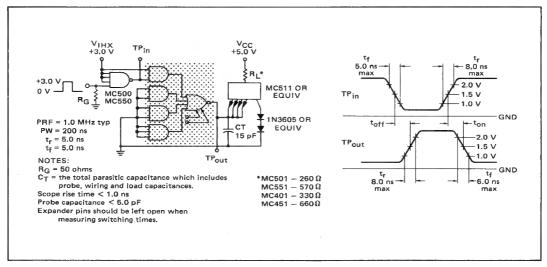
11 = (14 • 1) + (2 • 3) + (5 • 6) + (7 • 8 • 9) + (Expanders) Negative Logic:

11 = (14+1) • (2+3) • (5+6) • (7+8+9) • (Expanders)

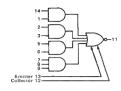
Total Power Dissipation = 30 mW typ/pkg Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(lp:)	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC501 MC551	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC401 MC451	1	(~1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0 ⁰ to +75 ⁰ C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for one input of the device. To complete testing, sequence through remaining inputs in a similar manner.



	1						TE	ST CO	NDITIO	NS					
				mA							Volts				
(@ Test	ار	οι	Ic	Н	-	V	٧	V _p	V	V	v	V	v	V _{IHX}
Ten	nperature	Pr*	Std	Pr*	Std	l _{in}	VIL	V _{IH}	*R	Vth 1	V _{th 0}	1ua 1	'cc	V _{CCH}	TIHX
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
AC501*, MC551 ·	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	
AC401*, MC451	} +25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0		-

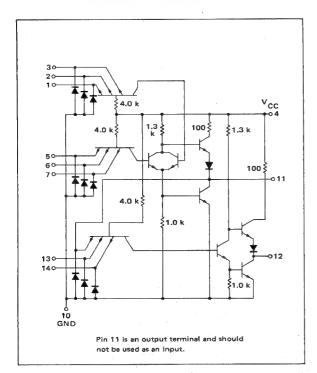
		,													+/3 C	20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1	0, 0	5,0			i I
		Pin			,	551 Te				AC401,							TEST CURF	RENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED	BELOW	<i>!</i> :		
		Under		55°C		25°C	_	25°C)°C		25°C	_	5°C	ļ	-		T .	· /	u.	v	v	W	l v	T _V	V	v	1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Пон	in	VIL	Viii	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}	V _{CCH}	VIHX	Gnd
Innut		T						1	T														Г	T	Ι			
Input Forward Current	$I_{\mathbf{F}}$	1	-	-1. 33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	14	-	-	_	4	-	-	1,2,3,5,6,7, 8,9,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1			-	4	-	-	2,3,5,6,7,8, 9,10,14
Inverse Beta Current	I,F	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
Breakdown Voltage	BV _{in"0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vde	-	-	1	-	-	-	٠	-	-	4	-	-	2,3,5,6, 7, 8, 9, 10
	BV _{in"1"}	1	5.5	-	5.5	-	5.5	-	5. 5	-	5. 5	-	5. 5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3.5.6, 7,8,9,10,14
Output Output Voltage	v _{out "0"}	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vde	11	-	-	-	-	-	1	-	-	4		-	2,3,5,6,7, 8,9,10
	V _{out "1"}	11	2.5	-	2. 4	-	2. 7	-	2.5	-	2. 4	-	2.5	-	Vdc	-	11	-	-	-	-	-	1	-	4	-	-	2,3,5,6,7. 8,9,10
Leakage Current	IOLK	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	11	4	-	-	1,2.3.5.6,7, 8,9,10.14
Short-Circuit Current	I _{SC}	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 5, 6, 7,8,9, 10,11,14
Output Voltage	V _{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
	v _{он}	11	2.8	-	3. 2	-	3. 35	-	3.0	-	3. 1	-	3. 15	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
Power Requirements			_																			1						
(Total Device) Maximum Power Supply Current	Imax	4	-	-	-	12	-	-	-	-	-	12	-	_	m Adc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6, 7,8,9,10,14
Power Supply Drain	I _{PDH}	4	<u> </u>	9.0	T-	9.0	1 -	9.0	-	11	1-	11	-	11	m Adc	-	-	-	-	-	-	-	-	-	4	-	-	10
	PDL	4	-	7. 5	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,9,10,14
Switching Parameters	<u> </u>		\vdash	†		_	_		\vdash		\vdash					Pulse In	Pulse Out								T			
Turn-On Delay	ton	1, 11	-	-	-	23	-	-	-	-	-	23	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Turn-Off Delay	toff	1, 11	-	-	-	23	-	-	-	-	-	23	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Rise Time	tr	1, 11	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Fall Time	t _f	1, 11	-		-	6, 0	-	-	-	-	-	6.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10

^{*} Prime Fan-Out.

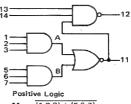
2-WIDE 3-INPUT "AND-OR-INVERT" GATE WITH GATED COMPLEMENT

MTTL MC500/400 series

MC503 · MC553 MC403 · MC453



This device is the only gate of the basic positive AND-OR-INVERT series that includes an additional 3-input AND-INVERT function on the output. This configuration provides the output and a gated complement in a single package. This device is useful in the design of adders, subtracters and one-shot multivibrators.



 $11 = \overline{(1\cdot 2\cdot 3) + (5\cdot 6\cdot 7)}$

12 = 11-13-14

 $12 = (1.2.3) + (5.6.7) + \overline{13} + \overline{14}$

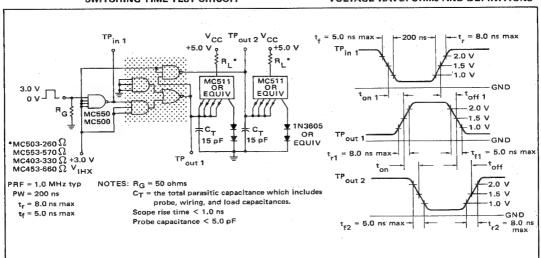
Total Power Dissipation = 35 mW typ/pkg Propagation Delay Times = 11 ns typ (Pin 1 to Pin 11) 10 ns typ (Pin 11 to Pin 12)

TRUTH TABLE

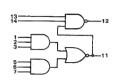
А	В	OUTPUT PIN # 11	PIN #13	PIN #14	OUTPUT PIN # 12
0	1	0	0	0	1
1	0	0	0	1	1
0	1	0	1	0	1
1	0	0	1	1	1
0	0 -	-1	0	0	1
0	0	1	0	1	1
0	0	1 .	1	, o	1 1
0	0	1	1	1	0

SERIES	INPUT LOADING FACTOR (IF)	OUTPUT DRIVE (IOL)	TEMPERATURE RANGE
MC503 MC553	1 (-1,33 mA)	15 MC500 Series Gates (20 mA) 7 MC500 Series Gates (10 mA)	-55°C to +125°C
MC403 MC453	1 (-1.66 mA)	12 MC400 Series Gates (20 mA) MC400 Series Gates (10 mA)	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the AND-OR-INVERT gate, plus one input of the gated complement. To complete testing, sequence through remaining inputs in the same manner.



							T	ST CO	NDITIO	NS					
				mA							Volts				
(@ Test	I,	DL.	I,	эн		v	v	V _R	v	v	v	v	v	v
Ter	nperature	Pr*	Std	Pr*	Std	lin	V _{IL}	VIH	*R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{ССН}	V _{IHX}
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	8.0	-
MC503*, MC553	+25°C	20	10	-1.5	-0.7	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	8.0	-
	(0°C	20	10	-1.2	-0.6	1, 0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	7.0	-
MC403*, MC453	} +25°C	20	10	-1. 2	-0.6	1.0	0.45	3.0	4. 5	1.8	1.2	5.5	5.0	7.0	3.0
	\ +75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-

			_												+/5 (20 10	-1.2 -0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-	
		Pin		MC503			_					53 Te]		TEST CUR	RENT	/ VOL	AGE A	APPLIED	TO P	INS L	STED	BELOW	1.		1
	l	Under	-	55°C	_	25°C		25°C	_	°C	_	25°C		5°C			1 .	1.					Т.					
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	I _{OH}	in	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input								Γ	Г	Ι	Γ		,		17	1		Т				ľ						
Forward Current	I_{F}	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3	-	-	-	4	-	-	1,5,6,7,10
		14	-	-1.33	-	-1.33	-	-1.33		-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	13	-	-	-	4	-	-	1,2,3,5,6, 7,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6, 7,10
		14	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	_	-	14	-	-	-	4	-	_	10,13
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAde	-	-	-	-	-	1	-	-	-	4	-		5,6,7,10
	_	14	-	100	-	100		100	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6, 7,10
Breakdown Voltage	BV _{in ''0''}	1	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-		5,6,7,10
		14	5.5	-	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	14	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10
	BV _{in} ''1''	1	5.5	-	5.5	-	5. 5	-	5.5	-	5. 5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,10
		14	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	14	-	-	-	-	-	-	4	-	-	10,13
Output Output Voltage	,,	11	_	0.45	_	0.45		0.45		0.45		0.45		0.45														
Output voltage	V _{out ''0''}	11 12	-	0.45		0.45	-	0.45	-	0.45	-	0.45	-	0. 45	Vdc	11	-	-	-	-	-	1	-	-	4		-	5,6,7,10
				0.45			_				_	0.45	-	0. 45	Vdc	12		_	_	-	-	14	_	-	4	-	-	1,2,3,5,6, 7,10
	v _{out "1"}	11	2.5	-	2.4	l .	2.7		2.5		2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	1	-	4	-	-	5,6,7,10
		12	2.5	-	2.4		2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	14	-	4	-	-	1,2,3,5,6, 7,10
Leakage Current	1 _O LK	11	-	1250	-	1250	-	1250	-	1250	-	1250	-	1250	μAdc	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6, 7,10
		12		250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-		_	-	-	-	-	12	4	_	_	10,13,14
Short-Circuit Current	ISC	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10,11
		12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10,12,13,14
Output Voltage	v _{OH}	11	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	-	5,6,7,10
		12	2.8	-	3.2		3.35	-	3.0		3.1	-	3.15	-	Vdc	•	12	-	14	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10
	V _{OL}	11	-	0.40		0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	- 1	-	-	4	-		5,6,7,10
		12	-	0.40	-	0.40	_	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	14	-	-	· -	-	4	-	-	1,2,3,5,6, 7,10

ELECTRICAL CHARACTERISTICS (continued)

							TE	ST CO	NDITIO	NS					
				mA							Volts				
	@ Test	ار	DL .	l _c	ж		٧ _{IL}	VIH	V _R	V _{th 1}	V _{th O}	Vout	V _{cc}	V _{CCH}	V _{IHX}
Ten	nperature	Pr*	Std	Pr*	Std	lin	. IF	* IH	*R	* th 1	* IH O	out	. 00	CCH	IIIA
1	_55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	8.0	-
MC503*, MC553	+25℃	20	10	-1.5	-0.7	1.0	0, 45	2. 8	4.5	1.7	1.2	5.5	5, 0	8.0	3.0
	(+125℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	8.0	_
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4. 5	1.9	1.1	5.5	5.0	7.0	-
MC403*, MC453	{ +25℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4. 5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-
3. MC453 Test Limits				TEST	CUR	PENT	/ VOLT	AGE A	PPLIED	TO P	INS 11	STFD I	BELOW		

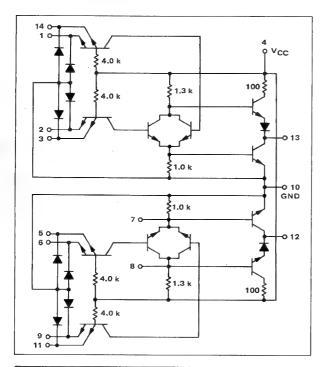
											u water decree				+/3 C	20 10	-1.2 -0.0	1.0	0.70	3.0	4. 3	1. 7	4.4	0.0	0	11.0		
		Pin				53 Te				C403,							TEST CURI	RENT ,	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED	BELOW	' :		
Characteristic	Symbol	Under Test		5°C Max		25°C Max		25°C Max		°C Max		25°C Max		5°C Max	Unit	lor	ОН	l _{in}	V _{IL}	V _{tH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V _{cch}	V _{IHX}	Gnd
CHOLOGICATORIO		1001	144111	77107		11107	1											=				-	7					
Power Requirements (Total Device)																		!										
Maximum Power Supply Current	I _{max}	4	-	34	-	34	-	34	-	24	-	24	-	24	mAde	-	-	-	-	-	-	-	-	<u> </u>	<u> </u>	4	-	1,2,3,5,6 7,10,13,1
Power Supply Drain	I _{PDH}	4	-	10	-	10	-	10	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-		-	4	-	-	10
	I _{PDL}	4	-	10	-	10	-	10	-	12	-	12	-	12	mAdç	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6 7,10
		4	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6 7,10,13,1
Switching Parameters					\vdash		_		┢							Pulse In	Pulse Out											
Turn-On Delay	ton 1	1, 11	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	ton 2	11, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Turn-Off Delay	toff 1	1, 11	-	-	-	22	-	-	-	-	-	22	1-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	t _{off 2}	11, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Rise Time	t _{r 1}	1, 11	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	t _{r 2}	11, 12	-	-	-	8. 0	-		-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Fall Time	t _{f1}	1, 11	-	-	-	6. 0	-	-	-	-	-	6.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	t _{f2}	11, 12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10

^{*} Prime Fan-Out

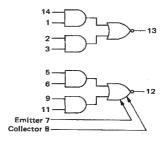
MTTL MC500/400 series

EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MC520 · MC570 MC420 · MC470



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC509 or MC510 expander series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.

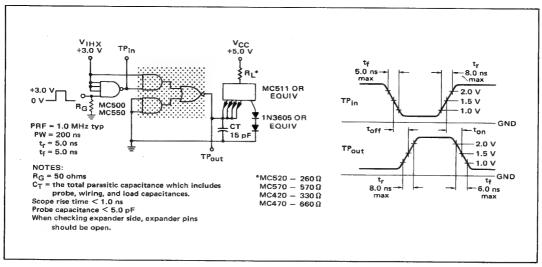


Positive Logic: $13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$ $12 = \overline{(5 \cdot 6) + (9 \cdot 11) + (Expander)}$

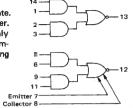
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC520 MC570	1	(-1.33 mA)	15 7	MC500 series Gates MC500 series Gates	 (20 mA) (10 mA)	-55°C to +125°C
MC420 MC470	1	(-1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	1						TE	ST CO	NDITIO	NS					
				mA							Volts				
(@ Test	ار)L	Ic	Н	l _{in}	٧	VIH	V _R	v	V _{sh 0}	٧.	V _{cc}	V _{CCH}	V _{IHX}
Ter	nperature	Pr*	Std	Pr*	Std	'in	*11.	тін	, "R	*th 1	* #6 0	* out	• 66	CCH	· IMA
	(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
MC520*, MC570	₹ +25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	(+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
MC420*, MC470	} +25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	(+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0		

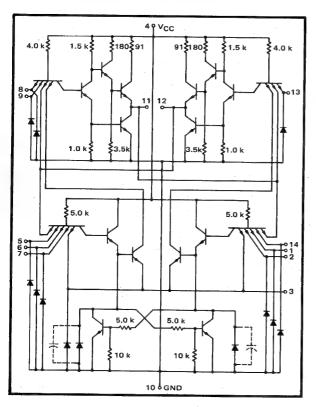
		Pin	М	C520,	MC5	70 Tes	st Lim	its		AC420,							TEST CURR	ENT,	/ VOLT	AGE A	PPLIED	TO P	ins li	STED I	BELOW	!:		
		Under		5°C	+2	5°C		25°C)°C	_	25°C	+7				1		V _{IL}	V _{IH}	V _R	V _{th 1}	v	V _{out}	V _{cc}	V _{cch}	V _{IHX}	Gnd†
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	OL	ІОН	in	V II.	* IH	*R	*161	V _{th0}	out	. CC	• ССН	- IHX	Ollu
Input Forward Current	$I_{ m F}$	1	- 1	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1, 66	mAdc		-	-	-	-	14	-	-	-	4	-	-	1,2,3,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,14
Inverse Beta Current	I_{L}	1	-	100	-	100	-	100	-	100	~	100	-	100	μAde	-	-	-	-	-	1	-	-	-	4	-	<u> </u>	2,3,10
Breakdown Voltage	BV _{in''0''}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	1	· -	1	_	-	-	<u> </u>	<u> </u>	<u> </u>	4	-	-	2,3,10
	BV _{in "1"}	1	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	_		4	-	L.	2,3,10,14
Output Output Voltage	v _{out "0"}	13	_	0. 45	_	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	13	-	-	-	-	-	1	-	-	4		-	2,3,10
Output voltage	Vout "1"	13	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	13	-	-	-	-	-	1	-	4	-	-	2,3,10
Leakage Current	IOLK	13	-	250	-	250	-	250	-	250	-	250	-	250	μAdc		-	-	-	-	-	-	-	13	4	-	-	1,2,3,10,14
Short-Circuit Current	I _{SC}	13	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	•	-	-	-	-	-	-	-	4	-		1,2,3,10, 13,14
Output Voltage	V _{OL}	13	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	13	-	-	-	1	-	-	-	-	4	-	-	2,3,10
Output Voltage	A OH	13	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	13	-	1	-	-	-		-	4	-	ļ <u>.</u>	2,3,10
Power Requirements (Total Device) Maximum Power Supply Current	Imax	4	-	-	-	10	-	-	-	-	-	10	-	-	mAde	-	-	-	-	-	-	-	-	-	- 4	4	-	1,2,3,10,14
Power Supply Drain	I _{PDH}	4	-	14		14	-	14	<u> </u>	18	<u> </u>	18	-	18	mAde		<u> </u>	-	<u> </u>	<u> </u>	-	<u>-</u>	1-	+-	4	+-	-	1,2,3,10,14
	I _{PDL}	4	-	7.0	-	7.0	-	7.0	-	8.0	-	8.0	-	8.0	mAde			_		Ĺ							ļ	1,0,0,0
Switching Parameters Turn-On Delay	ton	1,13	1_	_	_	22	_	_	_	_	_	22	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	4	-	14	2,3,10
	+	1,13	+-	+-	-	22	+-	+-	+	+-	+-	22	+-	+-	ns	i	13	-	-	-	-	1 -	1 -	† -	4	-	14	2,3,10
Turn-Off Delay	toff	1	+-		├ ─		-	 	-	+-	 - -	8.0	+-	+-	ns	1	13	+-	 - -	 -	-	+-	+-	+-	4	 -	14	2,3,10
Rise Time	tr	1,13	-		1	8.0	ļ-	_	\vdash	1-	-	1	<u> </u>	-	\leftarrow	1	13	-	-	+-	- -	+	╀.	+	4	+-	14	2,3,10
Fall Time	tf	1,13	-	-	1 -	6.0	-	-	-	-	-	6.0	-		ns	l	13	Ľ		<u> </u>	<u>. </u>					1		1

[†] Ground inputs to gates not under test during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

MTTL MC500/400 series

"AND" J-K FLIP-FLOP

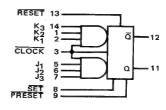
MC515 · MC565 MC415 · MC465



The MC415, MC465, MC515, and MC565 are clocked flip-flops that trigger on the negative edge and perform the J-K logic function. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct SET, PRE-SET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in the high state. When the clock goes low, the information is transferred to the bistable section and the Q and \overline{Q} outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct \overline{SET} , \overline{PRESET} , or \overline{RESET} inputs.

Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



	EQUIVALENT CIRCUIT	•	
SEŤ 80~ 90~ PRESET		1	0 13 RESET
J ₁ 5 0 1 2 6 0 1 3 7 0 1			0 14K3 0 1 K2 0 2 K1
V _{CC} = 4 GND = 10		Ţ	CLOCK

J	K	a _n	0 _{n+1}
0	0	0	0
0	0	1	1
0	1	0	o
0	1 1	1	0
1	0	0	1 1
1	0	1	lil
1	1	0	1
1	1	1	0
10/1			

Where $J = J_1 \circ J_2 \circ J_3$ $K = K_1 \circ K_2 \circ K_3$

Total Power Dissipation = 40 mW typ/pkg Switching Times:

ton = 25 ns typ toff = 13 ns typ

SERIES		OADING TOR	(1	F)			TEMPERATURE
0011120	CLOCK	ALL OTHER	CLOCK	ALL OTHER	OUTPUT DRIVE	(IOL)	RANGE
MC515 MC565	1.5	1	(-2.0 mA)	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates		~55°C to +125°C
MC415 MC465	1.5	1	(-2.5 mA)	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates		0°C to +75°C

MC515, MC565/MC415, MC465 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20ns.

Provides direct SET, PRESET, and RESET inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

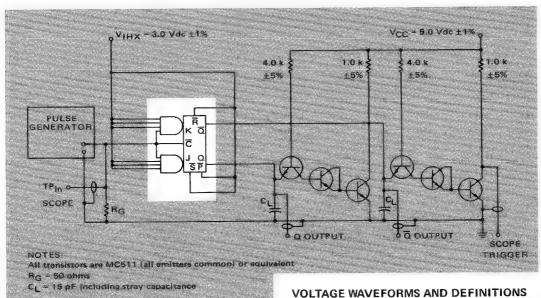
Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

state to "0" state information change on the J and K terminals. The flip-flop will require typically 10 ns to recognize ■ "0" state to "1" state change.

Negative edge triggering - When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and Q outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

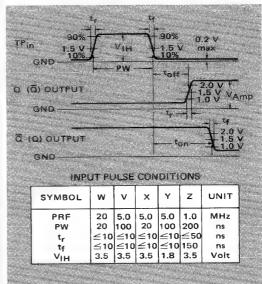
Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. \overline{PRESET} and \overline{SET} are tied to $\overline{\Omega}$; RESET is tied to Q.

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

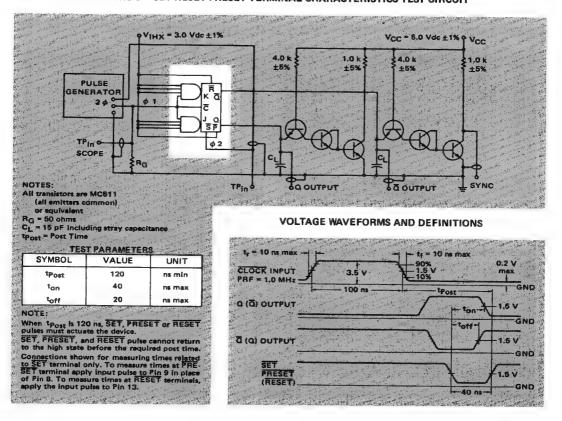
TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	toff	v		20	ns
Delay Time On	ton	V		40	ns
Rise Time	4 A 1	V		8.0	ns
Fall Time	t _f	V	they.	5.0	ns
Amplitude	VAmp	V V	3.2		Voit
(Device	WORST-C must toggle		300 ANAL 3	pulse)	
TEST	SYMBO	r, rimi	тѕ	CONDI	THE PERSON NAMED IN COLUMN TWO IS NOT
Toggle Frequenc	y frog	20 MH	zmax	V	
Pulse Width	PW	20 ms r	nin	×	
Input High Volt	age VIH.	1.8 V	min-		
Fall Time	4	150 ns	max	, z	7.7



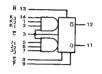
VIHX = 3.0 Vdc ±1% VEN/VINH VCC = 5.0 Vdc ±1% 4.0 k 1.0 k 40 4 1.0 k £5% ±5% ±5% PULSE GENERATOR SCOPE RG & Q OUTPUT TU TUO D & RIGGER NOTES: All transistors are MC511 (all emitters common) or INPUT VOLTAGE WAVEFORMS AND DEFINITIONS AG = 50 ohms OL = 15 oF including stray capacitan ENABLE MODE TEST: The device under test shall toggle when $V_{EN} = 1.8 \text{ Vdc} \pm 1\%$ is applied. INHIBIT MODE TEST: 1.5 V -10%_ The device under test shall NOT toggle who VINH = 1.2 Vdc ±1% is applied.

FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

FIGURE 3 - SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner,



								TES	T CON	IDITIONS				
				m/	1					٧	olts			
	@ Test	ا)L	l _c	ЭН						.,			
T _, e	mperature	Pr*	Std	Pr*	Std	lin	2 l _{in}	V _{IL}	V _{IH}	V _R	V _{th 0}	V _{th 1}	Vout	٧ _{cc}
	_55°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2. 0	5.5	5.0
MC515*, MC565	} +25℃	20	10	-1.5	-0.7	1.0	. 2. 0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	(+125°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0
	(°°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0
MC415*, MC465	} +25°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0
	(+75°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0

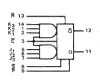
														_ (.	+75°C	20 10	-1.2 -0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0	
!	e S	Pin Under		иС515 5°С	-	565 Te 25°C		nits 25°C		MC415 °C					1		TEST CUI	RRENT	/ VOL	TAGE	APPLI	ED TO PINS	LISTED	BELOW	/:		
Characteristic	Symbol	Test								Max		5°C Max		5°C May	Unit	lor	Іон	l _{in}	2 I _{in}		V _{IH}	V _R	V _{th 0}			V _{cc}	Gnd
input Forward Current	I _F	1	-	-1.33	Т	-1. 33	T	-1.33	Γ	-1.66		-1.66	I		mAde		-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	- our	4	1,8,10
		5			-		-		-		-		-				-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-		5,10,13
		8	-		-				-		-		-					-		-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
		9	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-		9,10,13
		13	-	1	-	+	-	•	-	•	-	•	-	+	-	-	-	-		-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
Leakage Current	IR	1 5 8 9 13	-	100	-	100		100		100		100	-	100	μAdc	- - - -	-	1 1 1 1 1 1 1	-		-	1 5 8 . II 13	-	-	1 1 1	4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14 1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14 1,2,3,5,6,7,10,11,14
Inverse Beta Current	IL	1 5 8 9 13		100		100		100		100		100	-	100	μAdc	- - -	-			13	-	1 5 11 9	-		-	4	10
	BV _{in"0"}	8 9 13	5.5	1 1 1 1	5.5	1 4 4 1 1	5.5		5.5	-	5.5	1 1 1 1	5.5	-	Vdc	-	-	1 5 8 9		13	-	-	-	-	-	4	10
	BV _{in"1"}	1 5 8 9 13	5.5	7 - 2 - 5 -	5.5	-	5.5	- - -	5.5	-	5. 5	-	5.5		Vdc	-	- · ·	1 5 8 9		1 4 4 4 4	1 1 1 1	-	-	-	-	4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14 1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14 1,2,3,5,6,7,10,11,14

* Prime Fan-Out.

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



								TES	COND	ITIONS				
				m/						V	olts			
,	@ Test	ار)L	Ic	Н		2.1	v	v	V	V	v	v	V _{cc}
Ter	nperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	V _{IL}	VIH	V _R	V _{th O}	V _{th 1}	V _{out}	*cc
	(−55°C	20	10	-1.5	-0.7	1.0	2.0	0, 45	2.8	4.5	1.0	2.0	5.5	5.0
MC515*, MC565	+25°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2. 8	4. 5	1.2	1.7	5.5	5.0
	(+125°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4. 5	0.9	1.4	5.5	5.0
	(0°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4. 5	1,1	1.9	5.5	5.0
MC415*, MC465	{ +25℃	20	10	-1.2	-0.6	1.0	2.0	0.45	3. 0	4. 5	1.2	1.8	5.5	5.0
	(+75°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3. 0	4.5	1.1	1.7	5.5	5.0
E MCAGE Test Limit	le l													

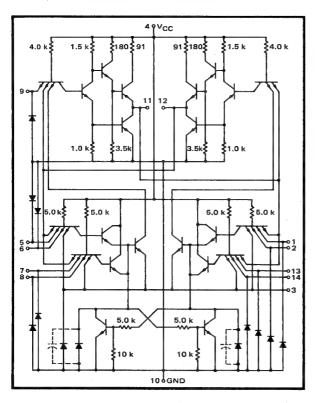
																					_						
		Pin				65 Te				ΛC4 15 °C		65 Te		nits '5°C			TEST CUI	RENT	/ VOL	TAGE	APPLI	ED TO PINS I	LISTED	BELOW	! :		
Characteristic	Symbol	Under Test	一55 Min			5°C Max		25°C Max				Max			Unit	lor	l _{on}	l _{in}	2 I _{in}	Λ ^{IF}	VIH	V _R	V _{th O}	V _{th 1}	Vout	V _{cc}	Gnd
Clock Input Forward Current	I _F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4	3,10
Leakage Current	I _R	3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-		3	-	-	-	4	1,2,5,6,7,10,14
Inverse Beta Current	IL	3 3	-	150 150	1 - 1	150 150	-	150 150	-	150 150		150 150	-	150 150	μAde μAde	-	- '	-	-	13 8	-	3 3	-	- -	-	4	10 10
Breakdown Voltage	BV _{in''0''}	3 3	5.5 5.5	-	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	Vdc Vdc	-	-	-	3 3	13 8	-	-	-	-	-	4 4	10 10
	BV in "1"	3	5.5	7-	5.5	-	5.5	-	5.5		5.5	-	5.5	-	Vdc		-	-	3	-		-	-	-	_	4	1,2,5,6,7,10,14
Output Output Voltage	v _{out "0"}	12 11 11	-	0.45	-	0.45	-	0.45	-	0.45		0.45		0.45	Vdc	12 11 11	-	-	-	-	-	-	-	13 9 8	-	4	3,8,10 3,10,13 3,10,13
	v _{out ''1''}	12 11 11	2.5	-	2.4	-	2. 7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12 11 11	-	-	-	-	- - -	13 9 8	-	1-	4	8,10 10,13 10,13
Leakage Current	IOLK	12 11	-	235 225	-	225 225	-	225 225	-	225 225	-	225 225	-	225 225	µAdc µAdc	-	-	-	-	-	-	-	-	-	12 11	4	1,2,3,5,6,7,8,9,10,13,14 1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I _{SC}	12 11	-	-	-45 -45	-90 -90	-	-	-	-	-45 -45	-90 -90	-	-	m Adc m Adc	-	-	-	-	-	-	-	-		-	4	1,2,3,5,6,7,8,9,10,12,13,1 1,2,3,5,6,7,8,9,10,11,13,1
Output Voltage	VOL	12 11 11	-	0.40	-	0.40	-	0. 45	-	0.40	-	0.40	-	0.45	Vdc 	12 11 11	-	-	-	-	13 9 8		-	-	-	4	3,8,10 3,10,13 3,10,13
	V _{ОН}	12 11	2.80	-	3. 20	-	3.35	-	3.00	-	3. 10	-	3.15	-	Vdc	-	12 11 11	-	-	13 9 8	-	-	-	-		4	8,10 10,13 10,13
Power Requirements (Total Device) Power Supply Drain	I _{PD}	4 4	-	12 12	-	12 12	-	12 12	-	14	-	14	-	14 14	m Ade	-	-		-	-		-	-	-	-	1-14 4	3,10,13 3,8,10

^{*} Prime Fan-Out.

MTTL MC500/400 series

"OR" J-K FLIP-FLOP

MC516 · MC566 MC416 · MC466

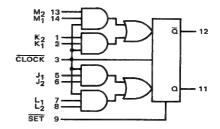


The MC516, MC566, MC416, and MC466 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct $\overline{\text{SET}}$ is also available.

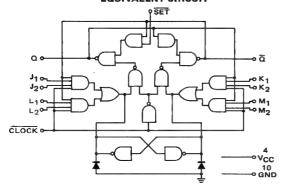
In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bistable section and the Q and the Q outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct SET input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.



EQUIVALENT CIRCUIT



J	L	К	М	an	Q _{n+1}
0	0	х	х	0	0
1	X	×	X	0	1
х	1	×	×	0	1
×	X	0	0	1	1
×	X	1	x	1	0
X	X	×	1	1	0

X = Don't Care Where J = J₁ • J₂ L = L₁ • L₂ K = K₁ • K₂ M = M₁ • M₂

Total Power Dissipation = 60 mW typ/pkg Switching Times: ton = 25 ns typ toff = 13 ns typ

SERIES		OADING TOR	(i _F)		OUTPUT DRIVE	(1)	TEMPERATURE
SERIES	CLOCK	ALL OTHER	CLOCK	ALL OTHER]	OUTFOT DRIVE	(IOL)	RANGE
MC516			(-4.0 mA)	(-1.33 mA)	15	MC500 series Gates	(20 mA)	=======================================
MC566	3		(-4.0 mA)	(-1.33 mA)	7	MC500 series Gates	(10 mA)	-55°C to +125°C
MC416	3		' (E O - A)	/ 1 SS A)	12	MC400 series Gates	(20 mA)	0°C to +75°C
MC466	3	1	(-5.0 mA)	(-1.66 mA)	6	MC400 series Gates	(10 mA)	0°C to +/5°C

MC516, MC566/MC416, MC466 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20 ns.

The application of a "0" state to the $\overline{\text{SET}}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering - When the clock goes from the high

state, the information in the temporary storage section is transferred; and the $\mathbb Q$ and $\overline{\mathbb Q}$ outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

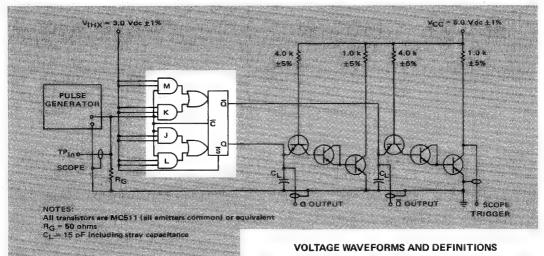
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

If both J, K, L, or M inputs are unused, they MUST be tied to ground.

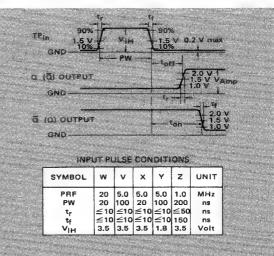
Unused \overline{SET} is tied to \overline{Q} .

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	toff	V		20	ns
Oeley Time On	ton	V		40	FYS
Rise Time		V		8.0	ns
Fall Time	man by	V	1004	5.0	ns
Amplitude	VAmp	V	3.2		Volt
(Device	WORST-CA must toggle v			pulse)	
TEST	SYMBOL	LIMI	TS	INP CONDI	
Toggle Frequenc	Y Yrog	20 MH	z mex	V	
Pulse Width	PW	20 ns	min	×	5.5
Input High Volt	age VIH	1.8 V n	nin-		
Fall Time		158 ns	max	2	



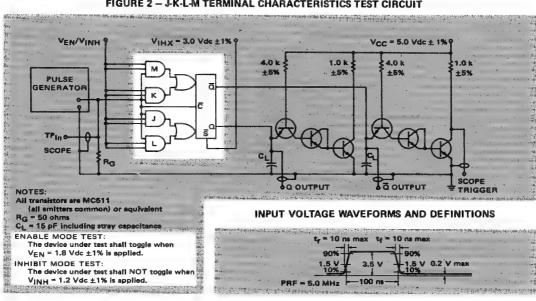
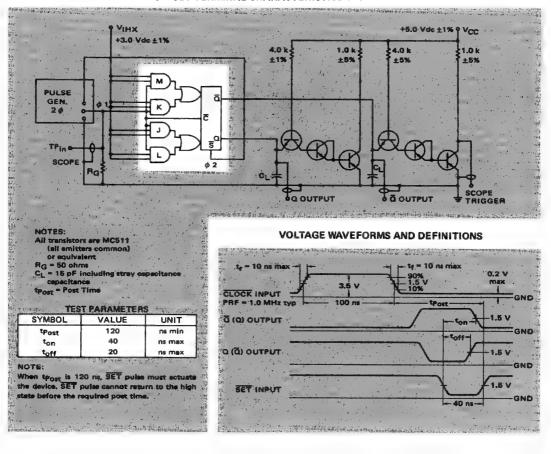
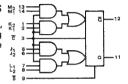


FIGURE 2 - J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT

FIGURE 3 - SET TERMINAL CHARACTERISTICS TEST CIRCUIT



ELECTRICAL CHARACTERISTICS Ma 13=



								TEST	COND	ITION	S				
					mA							/olts			
	@ Test	l _c	ML .	lo	Н						v				.,
Ter	nperature	Pr*	Std	Pr*	Std	lin	2 l _{in}	41 _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}
	_55°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
MC516*, MC566	+25°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4. 5	1.7	1.2	5.5	5.0
,	+125°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
	0°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
MC416*, MC466	+25°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5. 5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

														. (+75℃	20 10	-1.2 -0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5. 5	5.0]
		Pin			<u> </u>	66 Tes				MC416							TEST CUR	RENT	/ VOL	TAGE	APPLI	ED TO	PINS LIST	ED BEI	LOW:			
	1	Under	-5	5°C	+2	25°C	+1:	25°C	0	°C	+2	5°C	+7	5°C		· · · ·										1.4	1.4	-
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	1он	in	2 I _{in}	41 _{in}	ν _{IL}	V _{IH}	. V _R	V _{th 1}	Vmo	Vout	V _{cc}	Gnd
Input Forward Current	$^{1}\mathrm{_{F}}$	1	-	-1.33	,-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	-	2,3,5,6,7, 8,13,14	-	-	-	4	1,9,10
		5	-		- '		-		-		-		-			-	-	-	-	-	-	-	1,2,3,6,7, 8,13,14		-	-		5,10,11
		9	-		-		-	ļ	-	1	-	↓	-			-	-		-		-	-	1,2,5,6,7, 8,13,14	-	-	-	1	3,9,10,11
Leakage Current	I _R	1 5 9	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-		-	=	:	-		1 5 9	-	-	-	4	2,3,5,6,7,8,10,11,13,14 1,2,3,6,7,8,9,10,12,13,1 1,2,3,5,6,7,8,10,12,13,1
Inverse Beta Current	I _L	1 5 9	-	100	-	100	-	100	-	100	-	100	=	100	μAdc	-			-	-	-		1 5 9	-	-		1	9,10 10,11 10,11
Breakdown Voltage	вv _{in "0"}	1 5 9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1 5 9	-	-	-	-	-		-	-	4 	9,10 10,11 10,11
	BV _{in} "1"	5	5. 5	-	5.5	-	5.5	-	5.5	:	5.5	:	5. 5	-	Vdc	-	:	1 5 9	-	-	-	-	=	:	:	=	4	2,3,5,6,7,8,10,11,13,14 1,2,3,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,10,12,13,14

^{*} Prime Fan-Out

¹ Momentarily ground pin prior to taking measurement at terminal.

ELECTRICAL CHARACTERISTICS (continued)

				-				TEST	COND	ITION	IS				
					mA						1	√olts			
	@ Test	ار	DL .	ار	н								6		
Ter	nperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	4 I _{in}	VIL	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	Vcc
	(−55°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
MC516*, MC566	+25℃	20	10	-1,5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	(+125℃	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
	(0°C	20	10	-1,2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
MC416*, MC466	{ +25℃	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5. 5	5. 0
	(+75°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5 .	1.7	1.1	5.5	5.0

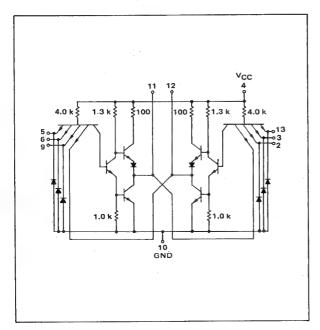
															7/3 C	20 10	-1.2 -0.6	1.0	2.0	4.0	0. 40	3.0	4.5 .	1.7	1.1	0.0	p. 0	
		Pin				566 Tes				MC416							TEST CHE	RRFNT	/ VOI	TAGE	ΔΡΡΙ	IFD T	O PINS LIST	TED RE	IOW.			
		Under	-5	5°C	+2	25°C	+13	25℃	0	°C	+2	25°C	+)	75°C	1		1201 001										,	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lou	Он	l _{in}	2 I _{in}	41 _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	Gnd
Clock Input Forward Current	I _F	3	-	-4.0	-	-4.0	-	-4.0	-	-5.0	-	-5.0	-	-5.0	mAdc	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	4	3,10
Leakage Current	I_R	3	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,8,10,13,14
Inverse Beta Current	IL	3	-	400 400	-	400 400	-	400 400		400 400	-	400 400	=	400 400	mAde mAde	-	-	-	-	-	-	-	3 3	-	-	-	4 4	9,10 10,11
Breakdown Voltage	BV _{in} "0"	3 3	5.5 5.5	- 1	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	Vdc Vdc	-	-	-	-	3	-	:	-	-	-	:	4	10, 11 9,10
	BV _{in"1"}	3	5.5	-	5.5	-	5.5	-	5.5	-	5. 5	-	5. 5	-	Vdc	-	-	-	3	-	-	-	-	-	-	-	4	1,2,5,6,7,8,10,13,14
Output (For Set Only) Output Voltage	v _{out "0"}	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	15 Vdc 11①		-	-	-	-	-	-	-	9	-	-	4	3, 10
	Vout "1"	11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	-	-	9	-	4	3,10
Leakage Current	IOLK	12 11	-	650 650	-	650 650	-	650 650	-	650 650	-	650 650	-	650 650	μAdc μAdc	-	-	-	-	-	-	:	12 11	-	-	-	4 4	1,2,3,5,6,7,8,10,11,13,14 1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I _{SC}	12 11	-	-	-45 -45	-90 -90	-	-	-	-	-45 -45	-90 -90	-	-	mAdc mAdc	-	_ :	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,10,11,12,13,14 1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	v _{он}	12 11	2.80 2.80	-	3.20 3.20	-	3.35 3.35		3.00 3.00		3.10 3.10	-	3.15 3.15	-	Vdc Vdc	-	12 11	-	-	-	-	-	-	-	-	-	4	3,10,11 3,10,12
	V _{OL}	12 11	-	0.40 0.40	-	0. 40 0. 40	-	0.45 0.45	1 1	0.40 0.40	-	0, 40 0, 40	-	0.45 0.45	Vdc Vdc	12① 11①	-	-	-	-	-	9	-	-	-	=	4	3,10 3,10
Breakdown Voltage	o ^I	12 11	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	mAdc mAdc	-	-	-	-	-	-	-	-	-	-	12 11	4	1,2,3,5,6,7,8,10,11,13,14 1,2,3,5,6,7,8,9,10,13,14
Power Requirements (Total Device)																												
Power Supply Drain	IPD	4	-	12	-	12 12	-	12 12	-	14	-	14	-	14	Vdc	-	-	-	-	-	-	-	-	-	-	-	4	3,10,12
	1PD	4		12		12	_	12	-	14		14		14	Vdc		-		-		-	-	-	-	-	-	4	3,10,11

^{*} Prime Fan-Out
① Momentarily ground pin prior to taking measurement at terminal.

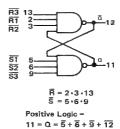
MTTL MC500/400 series

R-S FLIP-FLOP

MC513 · MC563 MC413 · MC463



This device consists of two independent dual 4-input NAND gates, internally cross coupled to realize a multiple input R-S flip-flop. The circuit can be used to eliminate switch contact bounce and to provide a temporary storage for data.



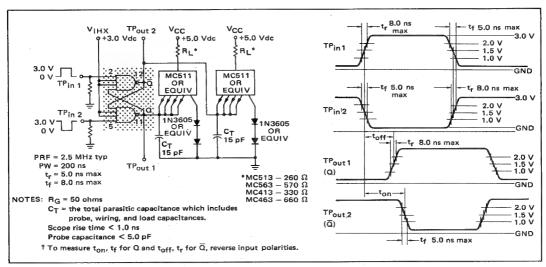
Total Power Dissipation = 30 mW typ/pkg Propagation Delay Time = 20 ns typ (to change state)

TRUTH TABLE (Positive Logic)

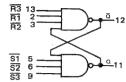
R	ŝ	Q	ā
0	0	Not Pe	rmitted
0	7	0	1
1	0	1	0
1	1	Q	₫

SERIES	INPUT LOADING FACTOR (IF)	П	OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC513 MC563	1 (-1.33 mA	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC413 MC463	1 (-1.66 mA	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0°C to +75°C

SWITCHING TIME TEST CIRCUIT †



Test procedures are shown for only one input. The other inputs are tested in the same manner.



								TI	ST CO	NDITIO	NS	·		
)o • ō 12					mA							Volts		
	(@ Test	10)L	Ic	H		· v	v	V	v	v	V.	Vcc
	Ter	nperature	Pr*	Std	Pr*	Std	'in	VIL	V _{IH}	V _R	V _{th} 1	V _{th 0}	Vout	*cc
)o		(−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5,0
	MC513*, MC563	} +25℃	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
		(+125℃	20	10	-1.5	-0,7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
		(0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1, 1	5.5	5.0
	MC413*, MC463	425°C	20	10	-1. 2	-0.6	1.0	0.45	3.0	4.5	1.8	1. 2	5.5	5.0
		(+75℃	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

	·	Pin				563 Te				AC413,						TEST	CURRENT / \	/OLT/	AGE AI	PPLIED	TO PI	NS LIS	TED BI	ELOW:		
		Under	_	55°C		25°C		25°C)°C	-	25°C		′5°C		-	· ·		,,	Ι.,	Τ.,	11/		.,	Lu .	1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	Іон	lin	V _{IL}	V _{IH}	· V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	Gnd
Input								100									[T				
Forward Current	$I_{\overline{F}}$	2 5	-	-1.33 -1.33	-	-1. 33 -1. 33	-	-1.33 -1.33		-1.66 -1.66		-1.66 -1.66		-1.66 -1.66		-	-	-	-	-	3,13 6,9	-	-		4	2,10 5,10
Leakage Current	I _R	2 5	-	100 100	-	100 100		100 100	-	100 100	-	100 100	-	100 100	μAdc μAdc	-	-	-	-	-	2 5	-	-	-	4	3,10,13 6,9,10
Inverse Beta Current	IL	2 5	-	100 100	-	100 100		100 100	-	100 100	-	100 100	-	100 100	μAdc μAdc	-	-	-	-	=	2 5	-	2	-	4 4	5,6,9,10 2,3,10,13
Breakdown Voltage	BV _{in''0''}	2 5	5. 5 5. 5	-	5. 5 5. 5	-	5. 5 5. 5	-	5.5 5.5		5. 5 5. 5		5. 5 5. 5	-	Vdc Vdc	-	-	2 5	-	-	-	-	-	-	4 4	5,6,9,10 2,3,10,13
	BV in "1"	2 5	5. 5 5. 5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	Vdc Vdc	-	-	2 5	-	-	-	-	-	-	4	3,10,13 6,9,10
Output Output Voltage	v _{out ''0''}	11	-	0.45	-	0.45	-	0.45	-	0. 45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	5	-	-	4	2,3,10,13
	Vout "1"	11	2. 5	-	2.4	-	2.7		2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-		-	5	-	4	2,3,10,13
Leakage Current	IOLK	11	- ,	1. 25	-	1. 25	-	1. 25	-	1. 25	-	1. 25	-	1. 25	mAdc		-	-	-	-	-	-	-	11	4	5,6,9,10
Short-Circuit Current	ISC	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAde	-	-	-	-	-	-	-	-	-	4	5,6,9,10,11
Output Voltage	VOH	11	2. 8	-	3. 2	-	3.35	-	3.0	-	3.1	-	3. 15	-	Vdc	-	11	-	5	-	-	-		-	4	2,3,10,13
	V _{OL}	11		0.40		0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	5	-	-	-	-	4	2,3,10,13
Power Requirements (Total Device)																										
Power Supply Crain	I _{PD}	4	-	-	-	9.0 9.0	-	-		-	-	9.0 9.0	-	-	mAde mAde	-	-	-	-	-	-	-	-	-	4	5,6,9,10 2,3,10,13
Switching Parameters	-			1												Pulse In	Pulse Out			_						
Turn-On Delay	t _{on} ‡	2, 12	<u> </u>	- :	-	30	-	-	-	-	_	30	-	-	ns	2, 5	12	۱- ـ	~	-	-	-	-	-	4	10
Turn-Off Delay	t _{off} ‡	2, 11	-		-	20	-	-	-	-	-	20	-	-	ns	2, 5	11	-	-	-	-	-	-	-	4	10
Rise Time	t _r ‡	2, 11		-	-	8.0	-	-	-	-	-	8.0	-	-	ns	2, 5	11	-	-	-	-	-	-	-	4	10
Fall Time	-t _f ‡	2, 12	-	-	-	5.0	-	-		-	-	5.0	-,,,	_	ns	2, 5	12	-	-	-	-	-	-	-	4	10

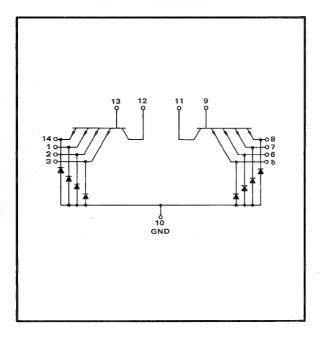
^{*} Prime Fan-Out

 $^{{\}bf 1}$ To measure ${\bf t_{on}},~{\bf t_{f}}$ for Q and ${\bf t_{off}},~{\bf t_{r}}$ for \$\overline{Q}\$, reverse input polarities.

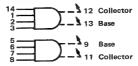
DUAL 4-INPUT EXPANDER FOR "NAND" GATES

MTTL MC500/400 series

MC511 · MC561 MC411 · MC461



This device consists of two independent 4-emitter input transistors, each of which performs the positive logic AND function when used in conjunction with expandable gates. The base and collector of each device is available for expansion. Using the MC511 with the MC506 expandable gate, the number of AND inputs can be expanded to 20.



Total Power Dissipation = 0 mW typ/pkg Propagation Delay Time: $\Delta t_{pd} = \pm 3.0 \text{ ns typ}$

When added to the expandable "AND-OR-INVERT" gate.

Δt_{pd}/pF = +1.6 ns/pF typ

Caused by additional capacitance at expander points.

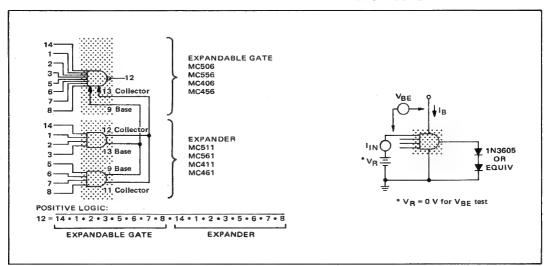
SERIES	INPUT LOADING (I _F) FACTOR	TEMPERATURE RANGE
MC511 MC561	1 (-1.33 mA)	-55°C to +125°C
MC411 MC461	1 (-1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION:

EXPANDABLE 8-INPUT "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

BVin "0", VBE, IL TEST CIRCUIT



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



				TEST CO	NDITIONS		
,	@ Test		mA			Volts	
	nperature	l ₈₁	I _{B2}	l _{in}	V _R	V _{DC}	٧ _c
	(−55°C	1.33	1.0	1.0	4.5	**	1.5
MC511 , MC561	\ +25°C	1.33	1.0	1.0	4.5	**	1.5
	(+125°C	1.33	1.0	1.0	4.5	**	1.5
	(0°C	1.66	1.0	1.0	4.5	**	1.5
MC411 , MC461	{ +25℃	1.66	1.0	1.0	4.5	**	1.5
	(+75°C	1.66	1.0	1.0	4.5	**	1.5

		Pin						t Limits MC411, MC461 Test Limits +125°C 0°C +25°C +75°C								TEST CUR	RENT / VO	LTAGE AP	PLIED TO I	PINS LISTE	D BELOW:	
al		Under		55°C		25°C							_	_			,		l v		· ·	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	¹ B1	B2	lin	V _R	V _{DC}	V _c	Gnd†
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAde	13	-	-	1	-	-	2,3,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	13	-	1	12	-	10
Breakdown Voltage	BV _{in ''0''}	1	5.5	-	5, 5	-	5.5	-	5. 5	-	5.5	-	5.5	-	Vdc	-	13	1	-	12	-	10
	BV _{in ''1''}	1	5. 5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	13	-	1	-	-	-	2,3,10,14
Base-Emitter Voltage	V _{BE}	13, 1	-	1.3	-	1, 1	-	1.0	-	1.3	-	1.2	-	1, 1	Vdc	13	-	-	-	12	-	1,10
Base-Collector Voltage	V _{BC}	13, 12		1.3	-	1.1	-	1.0	-	1.3	-	1.2	-	1.1	Vdc		13	-	-	-	-	10,12
Offset Voltage	v _o	12*	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	Vdc	13	-	-	-	-	- 1	1,10
Forward Beta	h _{FE}	12	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	-	13	-	-	-	-	12 ‡	1,10

[†] Ground inputs to expanders not under tests during ALL tests

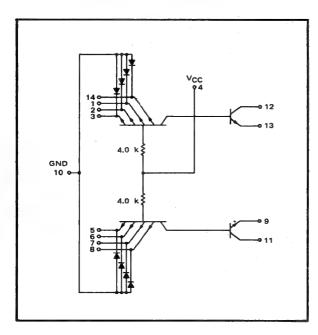
^{*} Measure VO from Pin 12 to gnd

^{**} Voltage obtained with two series diodes tied from collector to gnd. ‡ Measure I_C and calculate Beta. $\left(h_{FE} = \frac{I_C}{I_B}\right)$

DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL MC500/400 series

MC510 · MC560 MC410 · MC460



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC509 series and the MC510 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 10 mW typ/Pkg.

Propagation Delay Time:

Δt_{pd} = +1.0 ns typ When added to the expandable "AND-OR-INVERT" gate.

Δt_{pd}/pF = +1.0 ns/pF typ

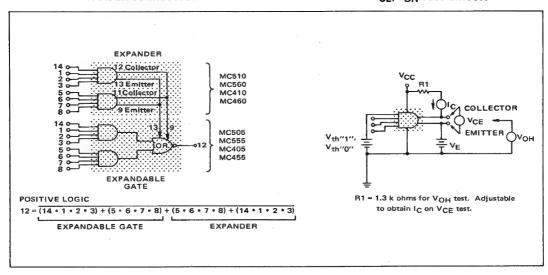
Caused by additional capacitance
at expansion points.

SERIES	INPUT LOADING (I _F) FACTOR	TEMPERATURE RANGE
MC510 MC560	1 (-1.33 mA)	-55°C to +125°C
MC410 MC460	1 (-1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

VCE, VOH TEST CIRCUIT



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



							TEST	CON	DITION	IS				
(@ Test	n	A						Volt	S				
	nperature	Ic	l _{in}	VR	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th O}	Vout	V _{CR}	V _{CRH}	V _{cc}	V _{CCH}
	(−55°C	4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*		5.0	-
MC510 , MC560	+25℃	4.0	1.0	4.5	0.85	0.75	0.8	1.7	1.2	5.5	*	**	5.0	8.0
	(+125℃	4.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	
	(0°C	4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-
MC410 , MC460	} +25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5.0	7.0
	(+75°C	4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*		5.0	-

		Pin				60 Tes				AC410,				_			T	EST CL	IRREN	T / VC	LTAGI	E APP	LIED T	O PIN	s list	ED BEL	OW:		
		Under		5°C		25°C		25°C)°C		25°C		′5°C		 	1			, 	,	r		_	,			V	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	l c	lin	V _R	V _{E1}	V _{E2}	V _{E3}	V _{th 1}	V _{th O}	Vout	V _{CR}	V _{CRH}	V _{cc}	V _{CCH}	Gnd [†]
Input																													
Forward Current	$\mathbf{I}_{\mathbf{F}}$	1	-	-1.33	-	-1.33	-	-1.33		-1.66	-	-1.66	-	-1.66	mAdc		-	2,3,14	-	-	-	-	-	-	-	-	4	-	1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	12	-	4	-	10
Breakdown Voltage	BV in "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	12	-	4	-	10
	BV in "1"	1	5. 5	-	5.5	-	5.5	-	5.5	-	5.5		5.5	-	Vdc	-	1	-	-	-	-		~	-	-	-	4	-	2,3,10,14
Output																													
Output Voltage	v _{OH}	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	13	-	-	1	-	12	-	4	-	10
	v _{CE} ①	12	-	0. 65	-	0.65	-	0.65	-	0, 65	-	0. 65	-	0. 65	Vdc	12	-	-	13		-	1	-	-	-	-	4	-	10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14
Power Requirements																													
(Total Device) Maximum Power Supply Current	I _{max} ②	4	-	-		10	-	-	-	-	-	10		-	mAde	-	-	-	-	~	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,14
Power Supply Drain	I _{PDH}	4	-	2.5	-	2.5	-	2.5		3.0	-	3.0	-	3.0	m.Adc	-	-	-	-	-	9,13	-	-	-	-	-	4	-	10‡
	I _{PDL}	4	-	3, 0	-	3.0	-	3.0	-	3.5	-	3.5	-	3.5	m Ade	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14

^{*} Indicated pins tied to V_{CC} thru 1.3 k ohms \pm 1.0% resistor.

^{**} Indicated pins tied to $V_{\rm CCH}$ thru 1.3 k ohms \pm 1.0% resistor.

[†] Ground inputs to gate not under test during ALL tests, unless otherwise noted.

I The inputs of both gates must be ungrounded.

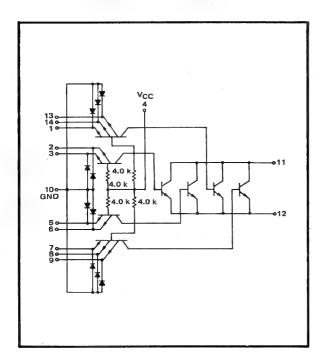
① VCE is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

²⁾ Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

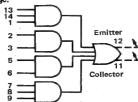
4-WIDE 3-2-2-3 INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL MC500/400 series

MC509 · MC559 MC409 · MC459



This device consists of two 2-input and two 3-input AND gates ORed together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC509 series or the MC510 series expander package.



Total Power Dissipation = 20 mW/pkg.

Propagation Delay Time:

$$\begin{split} \Delta t_{pd} = +4.0 \text{ ns typ (1.0 ns per ORed function)} \\ \text{When added to the expandable} \\ \text{"AND-OR-INVERT" gate.} \end{split}$$

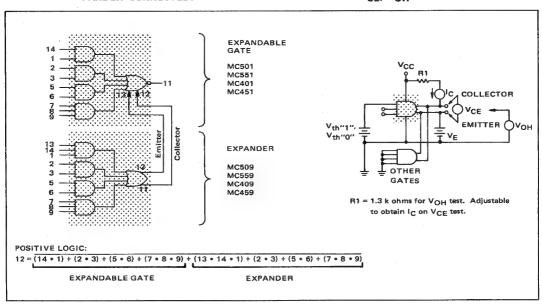
$$\begin{split} \Delta t_{pd}/pF &= 1.0 \text{ ns/pF typ} \\ &\quad \text{Caused by additional capacitance} \\ &\quad \text{at expansion points.} \end{split}$$

SERIES	INPUT LOADING (IF) FACTOR	TEMPERATURE RANGE
MC509 MC559	1 (-1.33 mA)	-55°C to +125°C
MC409 MC459	1 (-1.66 mA)	0°C to +75°C

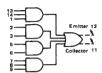
Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT"
GATE WITH A 4-WIDE 3-2-2-3 INPUT EXPANDER CONNECTED.

VCE, VOH TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



						T	est c	DNDIT	IONS					
	@ Test	m	A						Volts					
	mperature	lc	l _{in}	V_R	V _{E1}	V _{E2}	V _{E3}	V _{th 1}	V _{th 0}	$V_{\rm out}$	$V_{\rm CR}$	V_{CRH}	V _{cc}	V_{CCH}
	(55°C	4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*	- *	5.0	-
MC509 , MC559	} +25℃	4.0	1.0	4.5	0.85	0. 75	0.8	1.7	1, 2	5.5	*	**	5.0	8.0
	(+125℃	4.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
	(0°C	4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-
MC409, MC459	₹ +25°C.	4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5. 0	7.0
	(+75°C	4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*	-	5.0	-

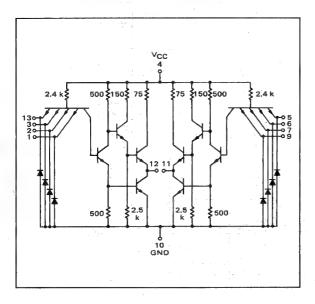
															.,,,														
		Pin		VIC509				_				59 Te					1	EST CURR	ENT /	VOLT	AGE A	PPLIE) TO F	PINS L	ISTED	BELOW	:		
		Under		5°℃		25°C		25°C		°C		25°C		5°C		<u> </u>						111	1/	11/	111		W	W.	١
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Ic	in	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	Vtho	Vout	V _{CR}	VCRH	V _{cc}	V _{CCH}	Gnd
Input Forward Current	I _F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-		2,3,5,6,7, 8,9,13,14		-	-	-	-	-	-	-	4	•	1,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	- 1	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	1	2,3,5,6,7,8, 9,10,13,14
Inverse Beta Current	I_{L}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV in "0"	1	5.5	-	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
	BV in "1"	1	5.5	-	5.5	-	5. 5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9, 10,13,14
Output	.,	11	4, 8	_	4.8		4.8		4.8	_	4.8	-	4.8	_	Vdc		_		,	12	_	_	1	_	11		4	P	2,3,5,6,7,8,9,10
Output Voltage	v _{oh} v _{ce} ①	11	4.6	0.65	4.8	0.65	4.0	0.65	4.0	0.65	4.0	0.65		0.65		11	-	-	12	-	-	1	_	-	-	-	4		2,3,5,6,7,8,9,10
Leakage Current	IOLK	11	-	250	-	250	-	250	-	250	-	250	-	250	μAde	-	-	-	-	-	12	-	-	11	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14
Power Requirements (Total Device) Maximum Power Supply Current	· I _{max}	4	-	-	-	20	-	-	_		-	20	-	-	mAde	-	-		-	-	12	-	-	-	-	11	-	4	1,2,3,5,6,7,8, 9,10,13,14
Power Supply Drain	I _{PDH}	4	-	5. 0 6. 0	-	5. 0 6. 0	-	5. 0 6. 0	-	6.0 7.0	-	6.0	-	6.0 7.0	mAdc mAdc	-	-	-	-	- -	12		-	-	-	-	4		10 1,2,3,5,6,7,8, 9,10,13,14

^{*} Indicated pins tied to V_{CC} thru 1.3 k ohms \pm 1.0% resistor. ** Indicated pins tied to V_{CCH} thru 1.3 k ohms \pm 1.0% resistor. ① V_{CE} is referenced to the emitter Voltage (Pin 12).

MTTL MC500/400 series

DUAL 4-INPUT LINE DRIVER

MC507 · MC557 MC407 · MC457



Each of the two independent drivers in the package consists of a 4-input AND gate driving an output inverter. The output inverter is capable of supplying twice the drive of the basic gates. The line driver is especially useful for driving high capacitive loads or for driving large fan-outs such as the numerous clock inputs of large counters.



Positive Logic: 12 = 1 • 2 • 3 • 13

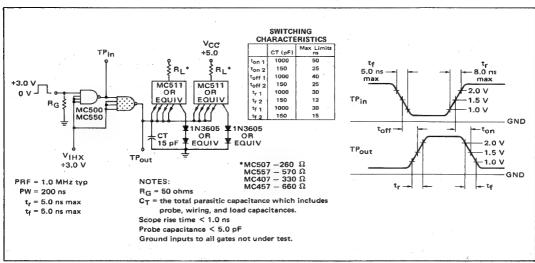
Negative Logic: 12 = 1 + 2 + 3 + 13

Total Power Dissipation = 60 mW typ/pkg Propagation Delay Time = 25 ns typ @ 1000 pF Load

SERIES	INPUT LOADING FACTO	R (IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC507 MC557	1.5	(-2.0 mA)*	30 15	MC500 series Gates MC500 series Gates		-55°C to +125°C
MC407 MC457	1.5	(-2.5 mA)*	24 12	MC400 series Gates MC400 series Gates		0°C to +75°C

^{*}Use I_F value of gate being driven (-1.33 or -1.66) to calculate output drive capability of line driver.

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one device. The other device is tested in the same manner. Further, test procedures are shown for only one input of the device under test. To complete testing, sequence through remaining inputs.



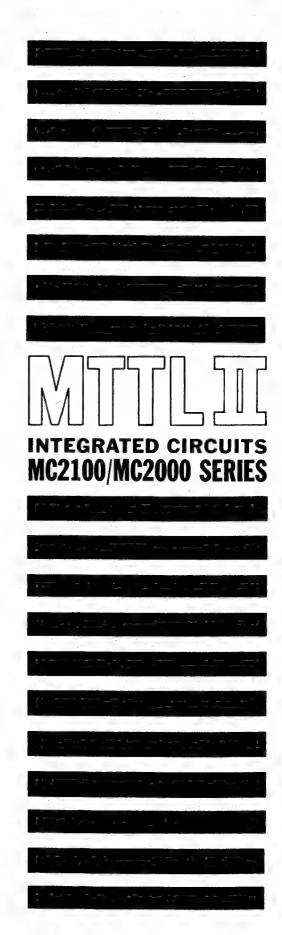
									rest co	ONDIT	ONS						
				mA							Volts						
	@ Test	10	DL.	ار	ЭН		V _{IL}	V _{IH}	V _R	V _{th 1}	٧.	ν.	V _{out 2}	۸ ^{or}	Vcc	V _{ccH}	V _{IHX}
Te	nperature	Pr*	Std	Pr*	Std	1in	*IL	*HH	*R	"th 1	*ih 0	*out 1	* out 2	, Or	, cc	*CCH	THX
	(−55°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	2.0	1.0	5.5	-	-	5.0	-	-
MC507*, MC557	425°C	40	20	-3.0	-1,5	1.0	0.45	2. 8	4.5	1.7	1.2	5.5	6.5	8.0	5.0	8.0	3.0
	(+125°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	1.4	0.9	5.5	-	-	5.0	-	-
	(0°C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.9	1.1	5, 5	-	-	5.0	-	-
MC407*, MC457	{ +25℃	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.8	1. 2	5.5	6.5	8, 0	5.0	7.0	3.0
	(+75°C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.7	1.1	5, 5	-	-	5. D	-	-
MC157 Tost Limits																	

															T/3 C	40 20	-2.4 -1.2	1.0	0.43	3.0	4.5	1.7	1.1	0.0		<u> </u>	0.0			4
		Pin		AC507						C407,							TES	T CU	RRENT	/ VOL	TAGE A	PPLIE	D TO I	PINS LI	ISTED B	ELOW	:			1
		Under		5°C		25°C_		25°C		°C		25℃		5°C	l			1	V	V	v	v	v	v	V	v	V	V _{CCH}	V	Gnd†
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Or	Іон	lin	V _{IL}	V _{IH}	V _R	V _{th 1}	Y th O	out 1	V _{out 2}	VOL	V _{cc}	₹ссн	V _{IHX}	Ondi
nput Forward Current	I _F	1	_	-2.0	_	-2.0	_	-2.0	_	- 2.5	-	-2.5	_	-2.5	mAde	-	-	_	-	_	2,3,13	_	-	_	_	_	4		-	1,10
Input Leakage Current		1	-	200	-	200	-	200	-	200	-	200	-	200	μAde	-	-	-	-	-	1	-	-	-	-	-	4	١.	-	2,3,10,13
Inverse Beta Current	I _I	1	-	200	-	200	-	200	-	200	-	200	-	200	μAde	-	-	-	-	-	1	-	-	-	-	-	4	-	-	10
Breakdown Voltage	BV _{in} 0	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	10
	BV _{in''1''}	1	5.5	-	5.5	-	5.5	-	5.5		5. 5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	2,3,10,13
Output Output Voltage	v _{out "0"}	12	_	0.45	_	0.45	_	0.45	_	0. 45	_	0.45	-	0. 45	Vdc	12	-	-	_	_	_	1	_	Ī.	_	-	4	_	-	10
	Vout "1"	12	2. 5	-	2.4	-	2.7		2. 5	-	2. 4	-	2. 5	-	Vde	-	12	-	-	-	-	-	1	-	-	-	4	-	-	10
Low Current MC507/407	I _{OL}	12	_	-	100	-	-	-	-	-	100	-	-	-	mAde	-	-	-	-	-	_	-		-	_	12	4.	-	_	10
MC557/457	OL.	12	-	-	60	-	-	-	-	-	60	-	-	-	mAde	-	-	-	-	-	-	-	-	-	-	12	4	-	-	10
Breakdown Current	I _O	12	-	-	-	1.0	-	-	-	-	-	1.0	-	-	mAde	-	-	-	-	-	-	-	-	-	12	-	4	-	-	1,2,3,10,13
Leakage Current	I _{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	-	-	4	-	-	1,2,3,10,13
Short-Circuit Current	I _{SC}	12	-50	-150	-50	-150	-50	-150	-50	-150	-50	-150	-50	-150	m Ade	-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10,12,1
Output Voltage	V _{ОН}	12	2.8	-	3. 2	-	3.35	-	3.0	-	3.1	I	3. 15	1	Vdc	-	12	-	1	-	-	-	-	-		<u> </u>	4	-	-	10
	VOL	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	-	-	4	-	-	10
Power Requirements Total Device)																	:													
Maximum Power Supply Current	I _{max}	4	-	-	-	15	-	-	-	-	-	15	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	-	4	-	1,5,10
Power Supply Drain	I _{PDH}	4	-	28	-	28	-	28	-	34	-	34	-	34	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I _{PDL}	4	-	9	-	9	-	9	_	11	-	11	-	11	mAde	-	-	-	-	-	-	-	-	-	-	<u> </u>	4	-		1,5,10
witching Parameters												50 I				Pulse In	Pulse Out	-									4		2,3,13	10
Turn-On Delay	t _{on} ①	1,12	-	-	-	50 ①	<u></u>	-	<u> </u>	-	-	1	1	-	ns	1	12	_		-	-	-	-	-	<u> </u>	-	<u> </u>	ļ-		<u> </u>
Turn-Off Delay	t _{off} ①	1,12	-	-	-	40 ①		-	·	-	-	40 Œ	1	-	ns	1	12	_		-	ļ -	-	_	_	ļ-	-	4	<u> </u>	2,3,13	10
Rise Time	t _r ①	1,12	-	-	-	30 ①		-	-	-	-	30 I	L	-	ns	1	12		-	-	-	-	-	-	-	_	4	-	2,3,13	10
Fall Time	t, ①	1,12	-	-	-	30 I	-	-	-	-	-	30 Œ	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10

^{*} Prime Fan-Out.

[†] Ground inputs to gates not under test during ALL tests, unless otherwise noted.
‡ The inputs to all gates must be ungrounded.

¹ Values @ 1000 pF load.



INTEGRATED CIRCUITS

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FLIP-FLOPS

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MC2110,2160/MC2010,2060

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MC2102,2152/MC2002,2052

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	O LOUGH AND OR INIVER	T Coto	171

2-Input AND-OR-INVERT Gate

AND J-K Flip-Flop

Dual 4-Input Expander for

AND-OR-INVERT Gates

AND-OR-INVERT Gates

4-Wide 3-2-2-3 Input Expander for

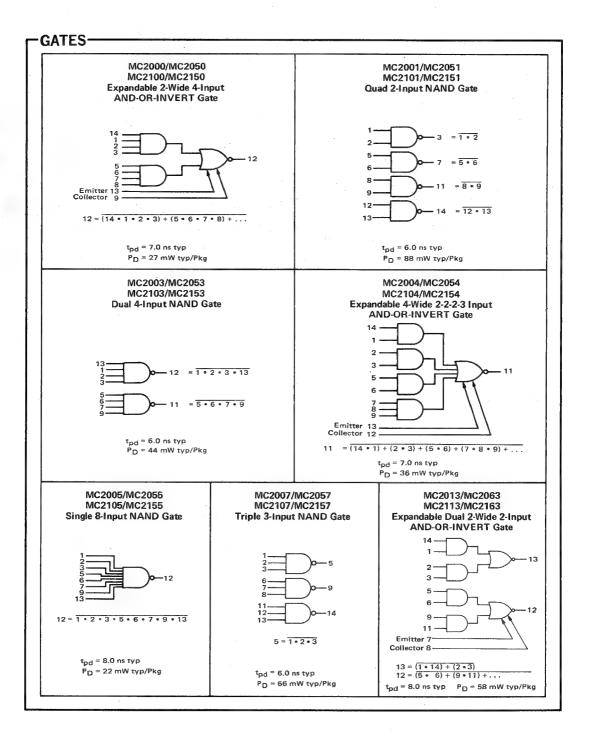
OR J-K Flip Flop

NUMERICAL INDEX (Functions and Characteristics)

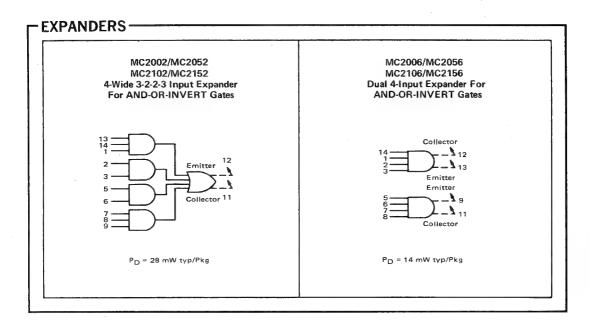
 $V_{CC} = 5.0 \text{ Vdc}, T_A = 25^{\circ} \text{C}$

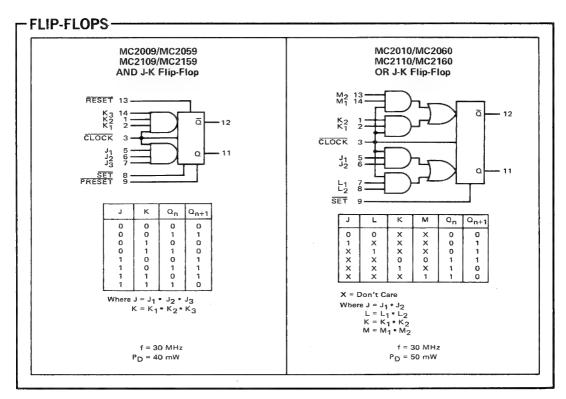
	T	ype	Out	put	Propagation	ļ	
Function	Case 609, 93	Case 609	Fac	ding tor Output	Delay ^t pd	Power Dissipation mW	Page No.
	0 to +75°C -55 to +125°C		MC2000 Series	MC2100 Series	ns typ	typ/pkg	
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LOGIC DIAGRAMS



LOGIC DIAGRAMS (continued)







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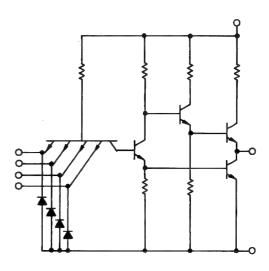
INTRODUCTION

MTTL II transistor-transistor logic is a high-speed, highnoise-immunity family of saturating integrated logic circuits.

The MTTL II family provides a speed extension of the medium-speed MTTL family. The circuits in the MTTL II family are identified by a multiple emitter input transistor and a two-stage active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The two-stage output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1-TYPICAL MTTL II CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous MC2100 Series MC2000 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
nput Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC2100 Series MC2000 Series	-55 to +125 0 to +75	°c
Storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°c
Maximum Junction Temperature MC2100 Series MC2000 Series	+175 +150	°c
Fhermal Resistance - Junction To Case $(heta_{ m JC})$ Ceramic Flat Package Plastic Dual-In-Line	0.09 0.15	°C/mW
Fhermal Resistance - Junction To Ambient ($\theta_{ m JA}$) Ceramic Flat Package Plastic Dual-In-Line	0.26 0.30	°C/mW



GENERAL INFORMATION SECTION

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL It family. Unless otherwise indicated, the Switching Threshold = 1.5 volts nominal parameters are defined for VCC = +5.0 volts and TA = +25°C High State = 400 k ohms nominal Low State = 2.5 k ohms nominal Supply Voltage Operating Range = 4.5 to 6.0 volts Worst-Case DC Noise Margin Operating Temperature Range: MC2100/2150 Series = -55 to +125°C MC2100/2150 series 0.700 volt minimum High State -MC2000/2050 series 0.600 volt minimum MC2000/2050 Series = 0 to +75°C MC2100/2150 series 0.650 volt minimum **Output Drive Capability** Low State - MC2000/2050 series 0,650 volt minimum Other Gates (Output Loading Factor): MC2100 Series = 11 MC2100 or MC2150 Series Gates. **Power Dissipation** MC2150 Series = 6 MC2100 or MC2150 Series Gates. MC2000 Series = 9 MC2000 or MC2050 Series Gates. MC2050 Series = 5 MC2000 or MC2050 Series Gates. 22 mW per gate typical 40-50 mW per flip-flop typical Switching Speeds(1) Capacitance = 600 pF Average Propagation Delay = 6.0 ns per gate typical 15 ns per flip-flop typical Output Impedance High State = 10 ohms (unsaturated) nominal Rise Time = 1.0 ns typical Low State = 10 ohms nominal Fall Time = 1.3 ns typical Output Valtage Swing = 0.2 to 3.5 volts typical Flip-Flop Clock Frequency (MC2109/MC2110 Series) = 30 MHz maximum. Input Voltage Limits +5.5 volts maximum 0.5 volt minimum

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL II gate is in the range of $10^7~{\rm A/s}$ and $10^8~{\rm V/s}$ respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL II circuits. A comparatively large, low-inductance type capacitor (in the 1.0 µF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 µF capacitors for every five packages throughout a breadboard is adequate to supress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving alarge capacitive load.

Power Dissipation

The standard supply voltage of the MTTL II logic circuits is +5.0 Vdc.The typical average dc power dissipation is given for each MTTL II circuit. (2) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.7 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL II circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL II logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical "1" level for the high state output loading is summarized for VCC = 5.0 V, VIL = 0.45 V and $I_{\rm OH} = -5.0$ mA:

MC2100/2150 Series - V_{OH} = 2.7 volts minimum @ -55°C MC2000/2050 Series - V_{OH} = 2.9 volts minimum @ 0°C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL II AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 0.7 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL II logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL II family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC2109/MC2110 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition require 300 ns settling time.

require 300 ns settling time.

The direct SET, PRESET, and RESET inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct SET, PRESET, and RESET inputs do not



GENERAL INFORMATION SECTION

override the clock and will not control the state of the flip-flop until 100 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 30 MHz
Maximum clock fall time	= 100 ns
Minimum clock pulse width	= 15 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= -0.5 V

Note: These boundary conditions for operation are not defined as occuring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the restriction of the clock fall time. If the clock fall time is greater than 100 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 30 MHz as long as the clock fall time is less than or equal to 100 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to -0.5 volt.

(1)The switching characteristics of the MTTL II family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turnon delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2}$$
 ns.

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where IpDL and IpDH are the typical dc current drains at VCC = +5.0 V.

MC2000/2050 and 2100/2150 MTTL II* series integrated circuits are electrically interchangeable with SUHL II† series logic circuits as shown in the cross reference below.

SG SF		-55 to	+125 ⁰ C	0 to -	+75°C		
NUMBER	Description	Fan-Out = 11	Fan-Out = 6	Fan-Out = 9	Fan-Out = 5		
SG210-213	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2100	MC2150	MC2000	MC2050		
SG220-223	Quad 2-Input NAND Gate	MC2101	MC2151	MC2001	MC2051		
SG230-233	4-Wide 3-2-2-3 Input Expander For AND-OR-INVERT Gates	MC2102	MC2152	MC2002	, MC2052		
SG240-243	Dual 4-Input NAND Gate	MC2103	MC2153	MC2003 MC205			
SG250-253	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2104	MC2154	MC2004	MC2054		
SG260-263	Single 8-Input NAND Gate	MC2105	MC2155	MC2005	MC2055		
SG270-273	Dual 4-Input Expander For AND-OR-INVERT Gates	MC2106	MC2156	MC2006	MC2056		
-	Triple 3-Input NAND Gate	MC2107	MC2157	MC2007	MC2057		
SF250-253	AND J-K Flip-Flop	MC2109	MC2159	MC2009	MC2059		
SF260-263	OR J-K Flip-Flop	MC2110	MC2160	MC2010	MC2060		
SG310-313	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2113	MC2163	MC2013	MC2063		

^{*}Trademark of Motorola In-

[†]Trademark of Sylvania Electric Products, Inc.



GENERAL INFORMATION SECTION

	DEFINITIONS	· te	Rice time
0V _{in} "0"	Input breakdown voltage (OM Isvel) Input breakdown voltage (OFF Isvel)	Δt _{pd}	Average increase in propagation delay per AND gate of expander when connected to an AND-OR-INVERT gate.
t _{Too}	Taggle frequency Collector current	Δι _{pd} /pF	increased propagation delay caused by additional capacitance at expension points.
Ig Ig	Input forward current	TPin	Test point at input of device under test
IFC	Forward current of clock input	TPout	Test point at output of device under test
I _{in}	Input current	VAmp	Voltage amplitude
2 In	2-times the Input Current	Voc	Power supply voltage
4 lin	4-times the Input Current	VCCH	High power supply voltage
h.	Inverse tota current	VCE	Collector-emitter voltage
LC	Inverse beta current of the clock input	VCR	Collector valuage obtained thru 1.3 k ohm retistor from VCC.
Imax	Maximum rated power supply current with V _{max} applied	VCRH	Collector voltage obtained thru 1.3 k ahm register from Voca.
10	Output broakdown current	VE1. VE2.	
lon	Output high current	VE3	Emitter voltage
iOL	Output low current	VEN	Enable voltage level
OLK	Output leakage current	VIH	Voltage for high input voltage state
ІРВН	Power supply drain with inputs high Power supply drain with inputs low	VIHX	Reduced supply voltage to hold input above three hold and to prevent noise from entering the device
PDL	Input reverse current with Va applied	VIL	Voltage for low input voltage state
IR Inc	Reverse current of clock input	VINH	Inhibit voltage level
Isc	Short circuit current obtained from device output	Vittax	Maximum rated gower supply voltage (VCC)
'SC	when one or more inputs are low	Voн	Output high voltage with IOH flowing out of pin
Pr	Prime Fan-Out	VOL	Output law voltage with IOL flowing into pin
PRE	Pulse repetition frequency	Vout "0"	Output low voltage with V _{th} -1- applied
PW	Pulse width	Vout "1"	Output high voltage with V _{th} "O" applied
Std	Standard for-out	VR	Imput reverse voltage
te	Fall time	V _{th} "0"	Input logic "O" threshold voltage
tott	Turn-off dalsy time	Water main	Input logic "1" threshold voltage

ton

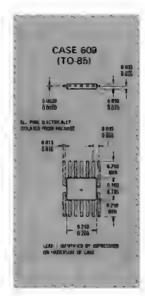
IPost

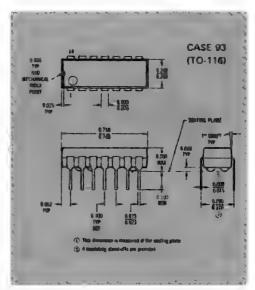
Turn-on delay time

The minimal time necessary before the SET, PRESEY, or RESEY inputs can control the flip-flop after the negative clock edge



All MTTL II integrated circuits are available in the TO-85 14-lead flat package MC2000 series is also available in the 14-lead dual in line plastic package, and selfin "F" to the beautype number to order plastic puckage, add selfin "F".

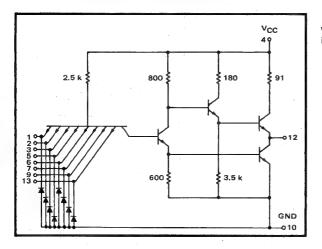




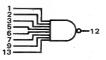
SINGLE 8-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2105 · MC2155 MC2005 · MC2055



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.

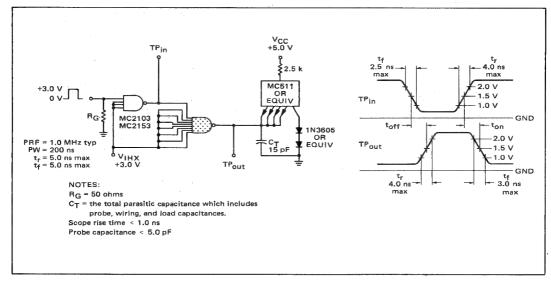


Positive Logic: 12 = 1 • 2 • 3 • 5 • 6 • 7 • 9 • 13 Negative Logic: 12 = 1 + 2 + 3 + 5 + 6 + 7 + 9 + 13

Total Power Dissipation = 22 mW typ/Pkg Propagation Delay Time = 8.0 ns typ

SERIES	INPUT LOADING FACTOR	(1 _E)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC2105 MC2155	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2005 MC2055	1	–2.5 mA	9 5	MC2000 series Gates MC2000 series Gates		0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



12

			TEST CONDITIONS																			
				mA							Volts											
	@ Test	I	OL .	l _o	н	1.	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	VIHX							
Ten	nperature	Pr*	Std	Pr*	Std	'in	•п.	, IH	. K	'th !	- III Q	out	- ((CCH	IIIA.							
	(−55°C	22.0	12.0	-2.2	-1.2	1,0	0.45	2.7	· 4.5	2.0	0.9	5.5	5.0		-							
MC2105*, MC2155	+25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0							
	(+125℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2. 7	4.5	1.4	0.9	5.5	5.0	-	-							
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-							
MC2005* MC2055	₹ +25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0							

MC2005*, MC2055

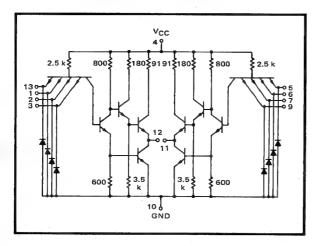
+75°C 22.5 12.5 -1.8 -1.0 1.0 0.45 2.9 1.7 1.0 5.5 4.5 MC2105, MC2155 Test Limits MC2005, MC2055 Test Limits TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: +25°C +125°C 0°C +25°C +75°C Under -55°C V_{CCH} V_{th 1} V_{th 0} ٧cc V_{iH} VIHX Gnd OL I_{OH} Min Max Min Max Min Max Min Max Min Max Min Max Unit Characteristic Symbol Test Input 4 1,10 -2.5 -2.5 2,3,5,6 -2.0 -2.0 -2.0 -2.5 mAdc Forward Current 7,9,13 100 100 4 2,3,5,6,7, Leakage Current 100 100 100 100 u.Adc 9,10,13 10 100 100 100 100 100 100 u Adc 1 4 Inverse Beta Current 1 BV_{in''0''} 10 5.5 1 4 5.5 5, 5 V dc Breakdown Voltage 5, 5 5.5 BV in "1" 4 2,3,5,6,7, 5,5 5.5 5.5 5, 5 5, 5 5.5 Vdc 9:10.13 Output 0, 45 10-0.45 0.45 0.45 0.45 _ 0.45 Vdc 12 Vout ''0" 12 Output Voltage 10-12 4 2.5 2.4 2.5 2.5 2.4 2.5 Vdc 12 V out ''1' 4 ,2,3,5,6,7 250 12 Leakage Current 12 250 250 250 250 250 u Adc IOLK 9,10,13 -100 -25 -100 -25 -100 -25 -100 -25 -100 mAdc 1,2,3,5,6,7 12 -25 -100 -25 Short-Circuit I_{SC} 9,10,12,13 Current 10 1 4 0.40 0.40 0.45 0.40 0.40 0.45 Vdc 12 12 Output Voltage VOL. 10 12 1 4 12 2, 70 3.10 3.15 2. 9 3.0 3.0 Vdc v_{oh} Power Requirements (Total Device) 4 1,10 6, 75 mAdc Maximum Power 6.50 Imax Supply Current 10 7.5 7.5 7.5 10 10 10 mAde Power Supply Drain IPDH 4 1.10 5.0 4 3.75 3.75 3.75 5.0 5.0 mAdc I_{PDL} Pulse In Pulse Out Switching Parameters 4 2,3,5,6 10 12 12 Turn-On Delay 1,12 12 ns 7,9,13 4 2,3,5,6 10 10 10 ns 1 12 Turn-Off Delay 1,12 toff 7,9,13 4 2,3,5,6 10 1 12 1,12 4.0 4.0 Rise Time tr 7,9,13 2,3,5,6, 10 12 3.0 3.0 ns 1 Fall Time tf 1,12 7,9,13

^{*} Prime Fan-Out.

DUAL 4-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2103 · MC2153 MC2003 · MC2053



This device consists of two 4-input NAND gates. The gates can be cross coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.

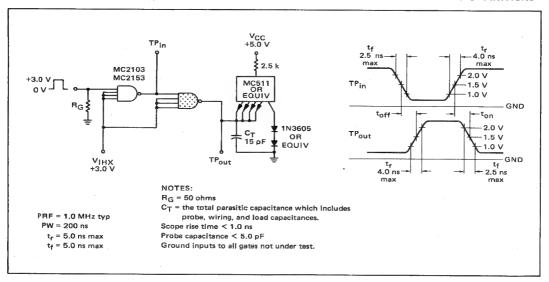


Positive Logic: 12 = 1 • 2 • 3 • 13 Negative Logic: 12 = 1 + 2 + 3 + 13

Total Power Dissipation = 44 mW typ/Pkg Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC2103 MC2153	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	55°C to +125°C
MC2003 MC2053	1	-2.5 mA	9 5	MC2000 series Gates MC2000 series Gates		0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. To complete testing, sequence through remaining inputs.



	1		TEST CONDITIONS												
			mA Volts												
	@ Test	ار	N.	I _{он}		٧ _{IL}	V _{IH}	V _R	V _{sh} 1	V _{th 0}	٧	Vcc	V _{CCH}	V _{IHX}	
Ter	nperature	Pr*	Std	Pr*	Std	lin	* IL	. 14	* K	mı	Thu	out	- 66	CCH	IHX
	(−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
MC2103*, MC2153	} +25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125℃	22.0	12.0	-2.2	-1.2	1.0	0, 45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2. 9	4.5	1.9	1.0	5.5	5.0	-	-
MC2003*, MC2053	} +25℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
MC2000 , MC2000	(+75℃	22.5	12.5	-1.8	-1.0	1,0	0.45	2.9	4.5	1.7	1.0	5.5	5.0		

	· · · · · ·	Di-	887	2103,	MCO	153 T	oet Li	mite	MC	2003	MC2	053 T	est li	mits			TEST CURR	ENIT	/ VOLT	ACE A	DDI IST	T∩ DI	INC I	ISTEN	RELOV	1.		
		Pin Under		.∠103, 5°C		5°C		25°C		°C		5°C	+7		- 1		1EST CORK	ENI /	VOLI	AUE A	FFLIED	יזעו	1142	13160	DLLOT			1 1
Characteristic	Symbol	Test	<u> </u>			Max						Max			Unit	loL	ОН	l _{in}	Vii	VIH	V _R	V _{th 1}	V _{th} (Vou	V _{cc}	V _{CCH}	V _{IHX}	Gnd [†]
input Forward Current	I _E	1	-	-2.0		-2.0	-	-2.0	-	-2.5	-	-2.5.	-	-2.5	mAdc		-	-	-		2,3,13	-	-		4	-	-	1,10
Leakage Current	I _R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-			4	-	· -	2, 3, 10, 13
Inverse Beta Current	I _L	1	-	100	-	100	-	100		100	-	100	-	100	μAdc	-	-	-	-	-	1	-	<u> </u>	-	4	-	-	10
Breakdown Voltage	BV _{in"0"} BV _{in"1"}	1	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	- -	5.5 5.5	-	5.5 5.5	-	V dc V dc	1 1	-	1	-	-	-	-	-		4	-	-	10 2, 3, 10, 13
Output Output Voltage	V _{out "0"} V _{out "1"}	12 12	- 2. 5	0.45	2.4	0.45	2.5	0.45	- 2. 5	0.45	- 2.4	0.45	2.5	0.45	Vdc Vdc	12 -	12	-	-	-	-	. 1	- 1	-	4 4	-	-	10 10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-		-	-		-	-	-	12	4		-	1, 2, 3, 10, 13
Short-Circuit Current	I _{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 10, 12, 13
Output Voltage	v _{OL}	12 12	2.70	0. 40	- 3. 10	0.40	3. 15	0.45	2.9	0. 40	3.0	0.40	3.0	0.45	V dc V dc	12	- 12	-	1	1 -	-	-	-	-	4 4	-	-	10 10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	13	-	-	_	-	-	13.5	-	-	m Ade	-	-	-	-		-	-	-	-	-	4	-	1,5,10
Power Supply Drain	I _{PDH}	4	-	15 7. 5		15 7. 5	-	15 7.5	-	20 10	-	. 20 10	-	20 10	mAdc mAdc	-		-	-	-	-	-	_	-	4	-	-	10 [‡] 1,5,10
Switching Parameters		 	+-:-			_	+-		\vdash	1	+					Pulse In	Pulse Out					Τ	T					
Turn-On Delay	ton	1,12	-	, -	-	10	-	-	-	-	-	10	-	-	ns	1	12	<u> </u> -	-	-	_	-	-		4	-	2, 3, 13	
Turn-Off Delay	toff	1,12	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	 	4	-	2, 3, 13	
Rise Time	tr	1,12	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns	1	12	-	-	-	<u> -</u>	-	-	-	4		2, 3, 13	
Fall Time	t,	1,12	-	1 -	-	2.5	-	-	-	-	T -	2.5	-		ns	1	12	-	-	1-	-	<u>l -</u>			4	<u> </u>	2, 3, 13	10

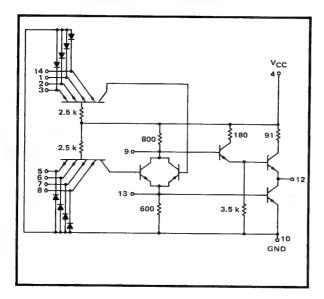
^{*} Prime Fan-Out.

[†] Ground inputs to gate not under test during ALL tests unless otherwise noted.

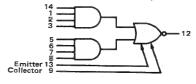
EXPANDABLE 2-WIDE 4-INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2100 · MC2150 MC2000 · MC2050



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds. This gate is usable for construction of half adders and other applications where the exclusive OR function is required.



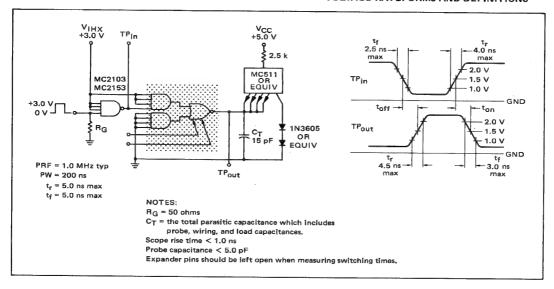
Positive Logic: 12 = (1 • 2 • 3 • 14) + (5 • 6 • 7 • 8) + (Expanders)

Negative Logic: 12 = (1 + 2 + 3 + 14) • (5 + 6 + 7 + 8) • (Expanders)

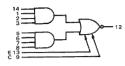
Total Power Dissipation = 27 mW typ/Pkg Propagation Delay Time = 7.0 ns typ

SERIES	INPUT LOADING FACTOR	(IE)		OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC2100 MC2150	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2000 MC2050	1 *	-2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining E18 inputs in the same manner.



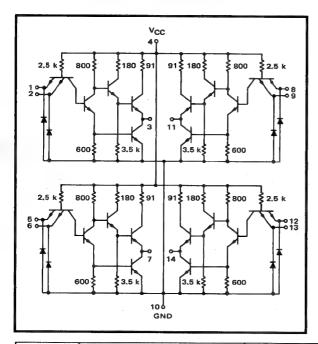
							TE	ST CO	NDITIO	NS					
			-	mA							Volts				
(@ Test	ار	DL .	lo	Н	ı	VIL	VIH	V _R	V,,, 1	V _{th 0}	Vout	ν _{cc}	V _{CCH}	V _{IHX}
Ten	nperature	Pr*	Std	Pr*	Std	1in	" IL	* IH	"R	*#h 1	* th 0	* out	. 66	- CCH	IHX
•	_55°C	22.0	12.0	-2. 2	-1.2	1.0	0.45	2. 7	4.5	2.0	0.9	5.5	5.0	-	-
MC2100*, MC2150	+25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0		
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2000*, MC2050	} +25℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	(+75℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	<u> </u>

		Pin				150 T					,	050 T					TEST CURR	ENT,	/ VOLT	AGE A	APPLIED	TO P	INS LI	STED	BELOW	/:		
Characteristic	Symbol	Under Test		5°C Max		5°C Max		25°C Max		°C Max		25°C Max		5°C Max	Unit	lot	ОН	l _{in}	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _F	1	-	-2.0	-	-2.0		-2.0	-	-2.5		-2.5	-	-2.5	m Adc	-	-	-	-	-	2,3,14	-	-	-	4	-	-	1,5,6,7, 8,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μ Adc	-	-	-	-	-	1	-	-	-	4	-	-	5, 6, 7, 8, 10
Breakdown Voltage	BV _{in"0"} BV _{in"1"}	1	5.5 5.5	-	5. 5 5. 5	-	5. 5 5. 5	-	5.5 5.5	-	5.5 5.5	1	5, 5 5, 5	-	Vdc Vdc	-	-	1	-	-	-	-	-	-	4	-	1	5, 6, 7, 8, 10 2, 3, 5, 6, 7, 8, 10, 14,
Output Output Voltage	v _{out"0"} v _{out"1"}	12 12	2. 5	0.45	2.4	0.45	2.5	0.45	- 2.5	0. 45	2.4	0.45	- 2. 5	0.45	V dc V dc	12	12	-	-	-	-	1 -	- 1	-	4	-	1	5, 6, 7, 8, 10 5, 6, 7, 8, 10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μ Adc	-	-	-	-	-	-	-	-	12	4	-	-	1, 2, 3, 5, 6, 7, 8, 10, 14
Short-Circuit Current	I _{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	_	-	-	4	-	-	1, 2, 3, 5, 6, 7,8,10,12,14
Output Voltage	v _{OH}	12 12	2.70	0.40	3.10	0.40	3.15	0.45	2.9	0.40	3.0	0.40	3.0	0.45	V _e de V de	12	- 12	-	1	1	-	-	-	-	4	-	1	5, 6, 7, 8, 10 5, 6, 7, 8, 10
Power Requirements (Total Device) Maximum Power	I _{max}	4	-	-	_	10	-	-	-	-	-	11		-	mAde	-	-	_	-	-	-	-	-	-	-	4	-	1,2,3,5,6, 7,8,10,14
Supply Current Power Supply Drain		4	 -	9.0	+-	9.0	-	9.0	-	12	+-	12	-	12	mAde	-	-	-	-	-		-	-	-	4	-	-	10
Tower supply Simil	I _{PDL}	4	-	6.0	-	6.0	-	6.0	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 5, 6, 7, 8, 10, 14
Switching Parameters Turn-On Delay	ton	1,12	_	-	_	11	_	_	_	-	_	11	_	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	4	-		5,6,7,8,10
Turn-Off Delay	toff	1,12	-	 -	-	11	-	-	-	-	-	11	-	-	ns	1	12	-	-	-	-	-	_	Ē	4	-		5, 6, 7, 8, 10
Rise Time	t _r	1,12		-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	12	-	-	-	-	-	<u> </u> -	-	4	-		5, 6, 7, 8, 10
Fall Time	t,	1,12	Τ-	T -	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5, 6, 7, 8, 10

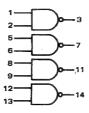
^{*}Prime Fan-Out.

QUAD 2-INPUT "NAND" GATE

MC2101 • MC2151 MC2001 • MC2051



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.

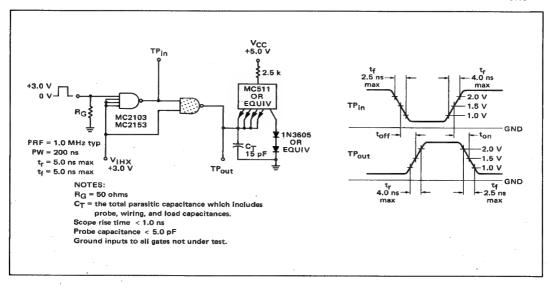


Positive Logic: $3 = 1 \cdot 2$ Negative Logic: 3 = 1 + 2

Total Power Dissipation = 88 mW typ/Pkg Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
MC2101 MC2151	1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	55°C to +125°C
MC2001 MC2051	1	-2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in a similar manner, Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



							TE	ST CO	NDITIO	NS					
				mA							Volts				
(@ Test	I _c	DL.	lo	Н		v	v	v	v	v	Vout	V _{cc}	v	v
Ter	nperature	Pr*	Std	Pr*	Std	l _{in}	۸ ^{II}	V _{IH}	V _R	V _{th 1}	V _{th 0}	a ont	*cc	V _{CCH}	V _{IHX}
	(−55°C	22.0	12.0	-2.2	-1.2	1,0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
MC2101*, MC2151	+25℃	22.0	12.0	-2.2	-1.2	1.0	0, 45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0		-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	_
MC2001*, MC2051	425°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	(+75℃	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

		Pin	M	C2101	, MC	2151 1	est L	mits	M	C2001	, MC	2051 1	est L	imits			TEST CURF	RENT	/ VOLT	AGF A	PPLIFD	TO P	INS LI	STFD	RFLOW	٠.		
		Under	-5	55°C	+:	25°C	+1	25°C	0)°C	+	25°C	+7	′5°C	1		1201 0011						_					4
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lot	I _{OH}	l _{in}	Vil	V _{IH}	V _R	Vihi	V _{th 0}	Vout	Vcc	V _{CCH}	V _{IHX}	Gnd [†]
Input				T						Ī	Ī													†				
Forward Current	$I_{\overline{F}}$	1	_	-2.0	-	-2.0	-	-2.0	l -	-2.5	-	-2.5	-	-2.5	mAde	-	-	-	-	-	2	-	-	-	4	-	-	1,10
Leakage Current	$^{\mathrm{I}}\mathrm{_{R}}$	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2, 10
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV in ''0''	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	 -	Vdc		-	1	-	-	-	-	-	-	4	-	-	10
	BV _{in"1"}	1	5, 5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2, 10
Output			_			1			-		_		 	 														
Output Voltage	v _{out "0"}	3	-	0.45	-	0.45	-	0.45	-	0.45	-	0. 45	-	0.45	Vdc	3	-		-	-	-	1	-	-	4	-	-	10
	v _{out ''1''}	3	2.5	-	2.4	-	2. 5	-	2.5	-	2.4	-	2.5	-	Vdc	-	3	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I _{OLK}	3	-	250		250	_	250	-	250	-	250	-	250	μAdc	-		-		-	-	-	-	3	4		-	1, 2, 10
Short-Circuit Current	ISC	3	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	1	-	-	-	4	-	-	1, 2, 3, 10
Output Voltage	v _{ol}	3	-	0.40	-	0.40	T -	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	_	-	-	1	-	-	-	-	4	-	-	10
	v _{oh}	3	2. 70	-	3. 10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	3	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device)																												
Maximum Power Supply Current	I _{max}	4	-	-	-	26	-	-	-	-	-	27	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,5,8, 10,12
Power Supply Drain	IPDH	4	T -	30	-	30	-	30	-	40	-	40	~	40	m Adc	-	-	-	-	-	-	_	-	-	4	-	-	10‡
	IPDL	4	-	15	-	15	-	15	-	20	-	20	-	20	m Adc	-	-	~	-	-	~	-	-	-	4	-		1,5,8, 10,12
Switching Parameters			_				 						i –			Pulse in	Pulse Out							_				10,12
Turn-On Delay	t _{on}	1,3	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Turn-Off Delay	toff	1,3	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Rise Time	tr	1,3	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Fall Time	t _f	1,3	-	-	-	2.5	-	-	-	-	-	2.5	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10

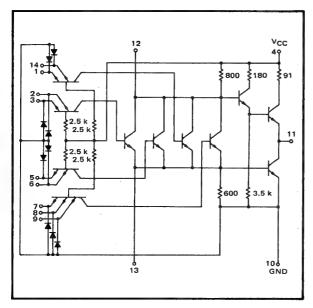
^{*}Prime Fan-Out

[†] Ground inputs to gates not under test during ALL tests unless otherwise noted. ‡The inputs of all gates must be ungrounded.

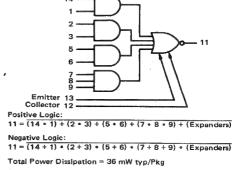
EXPANDABLE 4-WIDE 2-2-2-3 INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2104 · MC2154 MC2004 · MC2054



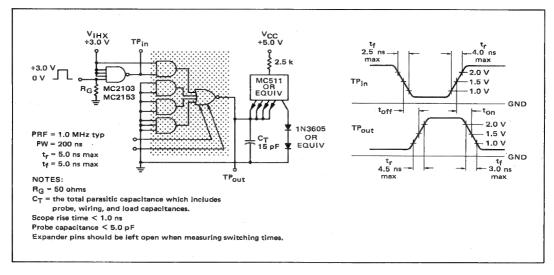
This device consists of three 2-input and one 3-input AND gates ORed together and driving an output inverter. The ORing nodes are made available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds.



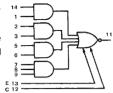
Propagation Delay Time = 7.0 ns typ

SERIES	INPUT LOADING FACTOR	(IF)		OUTPUT DRIVE	(1 _{OL})	TEMPERATURE RANGE
MC2104 MC2154	. 1	-2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	-55°C to +125™C
MC2004 MC2054	1	-2,5 mA	9 5	MC2000 series Gates MC2000 series Gates		0°C to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



<u> </u>	

@	Test
Temp	eratur

MC2104*, MC2154

			mA							Volts			
Test	I)L	10	н	l _{in}	٧,,	ViH	V _R	V _{th 1}	ν.	v	v	V _{CCH}
perature	Pr*	Std	Pr*	Std	'in	*11.	* IH	"R	*th 1	*th 0	Tout	*cc	*CCH
−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-
+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0
+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-
0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-
+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0
+75°C	22.5	19 5	-1 8	-1.0	1 0	0.45	2 0	4.5	1 7	1.0	6.5	5.0	

TEST CONDITIONS

VIHX

3.0

MC2004*, MC2054

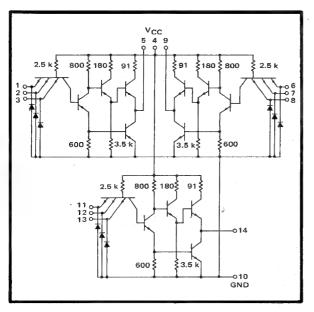
															T/3 C	22. 5 12. 5	-1.0 -1.0	1,0	0.40	2.9	4.0	1.7	1.0	3.3	1 3.0			
		Pin		C2104								054 T					TEST CURR	ENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED	BELOW	<i>l</i> :		
	١	Under	_	55°C		5°C		25℃		°C		25°C	_	5°C		1	1	1	V	v	V _R	v	v	v	v	V _{CCH}	V _{IHX}	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	lor	ОН	lin	V _{IL}	V _{IH}	V _R	V _{th 1}	V _{th 0}	V _{out}	V _{cc}	V CCH	YHX	Gnd
Input Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	14	-	-	-	4	-		1,2,3,5,6,7, 8,9,10
Leakage Current	I_{R}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-		2,3,5,6,7,8, 9,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
Breakdown Voltage	BV _{in''0''}	1	5, 5	-	5.5	-	5,5	-	5, 5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8, 9, 10
	BV _{in"1"}	1	5.5	-	5.5	-	5, 5	-	5.5	-	5. 5	-	5, 5		Vdc	-	-	1	-	-	-	-	-	-	4	-		2,3,5,6,7, 8, 9, 10, 14
Output Output Voltage	V _{out "0"}	11	-	0. 45	-	0. 45	-	0. 45	-	0. 45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	1	-	-	4	-	-	2,3,5,6,7, 8,9,10
	v _{out} ,.1	11	2. 5	-	2. 4	-	2.5	-	2 . 5	-	2.4	-	2.5	-	V dc	-	11	-	-	-	-	-	1	-	4	-	-	2,3,5,6,7, 8,9,10
Leakage Current	IOLK	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	11	4		-	1,2,3,5,6,7, 8,9,10,14
Short-Circuit Current	Isc	11	-25	-100	-25	-100	-25	-100	-25	-100	- 25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7, 8,9,10,11, 14
Output Voltage	v _O L	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-	-	2,3,5,6,7, 8,9,10
,	V _{OH}	11	2. 70	-	3. 10	-	3. 15	-	2.9	-	3. 0	-	3.0	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	- :	2,3,5,6,7, 8,9,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	17	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7, 8,9,10,14
Power Supply Drain	IPDH	4	-	12	-	12	-	12	-	16	-	16	-	16	mAde	-	-	-	-	-	-	-	-	-	4	-	-	10 1,2,3,5,6,7,
	IPDL	4	-	10	-	10	-	10	-	13	-	13	-	13	mAdc	-	-	_	-	Ī.	ļ -				7	_		8,9,10,14
Switching Parameters Turn-On Delay	t _{on}	1,11	-	-	-	12	-	-	-	-	-	12	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Turn-Off Delay	toff	1,11	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10
Rise Time	tr	1,11	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	11	-	-	-	-		-	-	4	-	14	2,3,5,6,7, 8,9,10
Fall Time	t _f	1,11	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7, 8,9,10

^{*} Prime Fan-Out.

TRIPLE 3-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2107 · MC2157 MC2007 · MC2057



This device consists of three 3-Input AND gates driving output inverters. These gates can be used to build a pulse shaping network for interfacing with discrete component circuits.

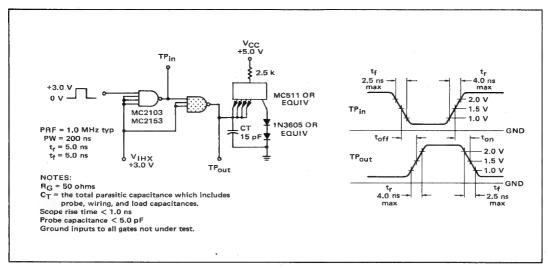


Positive Logic: $5 = \overline{1 \cdot 2 \cdot 3}$ Negative Logic: $5 = \overline{1 + 2 + 3}$

Total Power Dissipation = 66 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR	(IF)	OUTPUT DRIVE		(IOL)	TEMPERATURE RANGE
MC2107 MC2157	1	(-2.0 mA)	11 MC2100 series Gates 6 MC2100 series Gates	11 6	(22 mA) (12 mA)	-55°C to +125°C
MC2007 MC2057	1	(-2.5 mA)	9 MC2000 series Gates 5 MC2000 series Gates	A) 9 5	(22.5 mA) (12.5 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same manner, Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TE	ST CO	NDITIO	NS					
				mA							Volts				
	@ Test	١ _c	OL .	l _c	Н	l _{in}	٧	V _{IH}	V _R	V _{th 1}	V _{th 0}	Vout	V _{cc}	V _{CCH}	v
Ter	nperature	Pr*	Std	Pr*	Std	*in	, 1	*IH	*R	th 1	*th O	out	*cc	*CCH	V _{IHX} - 3.0 3.0
	(−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
MC2107*, MC2157	{ +25℃	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2007*, MC2057	{ +25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	(+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	3.0

MC2007*,	MC2057	1
		- (

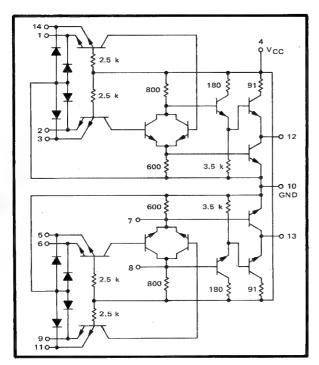
MC2107, MC2157 Test Limits MC2007, MC2057 Test Limits Pin TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: Under −55°C +25°C +125°C 0°C +25°C +75°C V_{th 7} V_{th 0} V_{out} Characteristic Symbol lou V_{CC} V_{CCH} V_{IHX} Test Min Max Min Max Min Max Min Max Min Max Min Max Unit I_{OH} Gnd† Input Forward Current -2.0-2.0 -2.0 -2.5 -2.5 -2.5 mAde 2,3 4 1.10 Leakage Current. I_R 100 100 100 100 100 100 μAdc 4 2,3,10 100 100 100 100 Inverse Beta Current 1 100 100 μAdc 1 10 IT. 4 BV in ''0" 5.5 5. 5 5.5 5, 5 5.5 5.5 1 Breakdown Voltage Vdc 4 10 BV_{in "1"} 5.5 5.5 5, 5 5.5 5.5 5.5 Vdc 1 4 2,3,10 Output Output Voltage 0.45 0.45 0.45 0.45 0.45 0.45 Vdc 5 4 10 Vout "0" 2.5 2.4 2,4 2.5 10 2.5 Vdc 5 V_{out "1"} Leakage Current 250 250 250 250 250 250 μAdc 5 4 1,2,3,10 IOLK -25 -100 -25 -100 mAdc Short-Circuit -25 -100 -25 -100 -25 -100 -25 -100 4 1,2,3, Current 5,10 Output Voltage v_{OL} 0.40 0.40 0.45 0.40 0.40 0.45 Vdc 5 1 4 10 3.0 10 2.7 3.1 3,15 2.9 3,0 4 1 V_{OH} Power Requirements (Total Device) Maximum Power 19.5 20, 25 mAdc 4 1,6,10,11 Imax Supply Current Power Supply Drain 4 22.5 22.5 22.5 30 30 '30 mAde 4 10 İ IPDH 1,6,10,11 11.25 11.25 15 15 15 mAdc 11.25 IPDL Switching Parameters Pulse in Pulse Out 10 Turn-On Delay 1,5 10 10 5 2.3 Turn-Off Delay 1,5 10 10 5 4 2,3 10 toff Rise Time 2,3 10 1,5 4.0 4.0 ns 1 5 1,5 10 Fall Time 2.5 2,5 2,3

^{*} Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

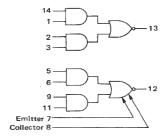
EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2113 • MC2163 MC2013 • MC2063



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC2102 or MC2106 expanders series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



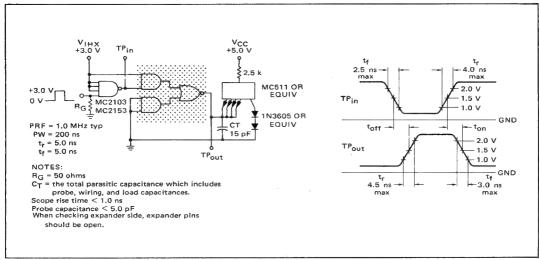
Positive Logic: $13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$ $12 = \overline{(5 \cdot 6) + (9 \cdot 11) + (Expander)}$

Total Power Dissipation = 58 mW typ/pkg Propagation Delay Time = 8.0 ns typ

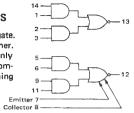
SERIES	INPUT LOADING FACTOR	(IE)		OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC2113 MC2163	1	(-2.0 mA)	11 6	MC2100 series Gates MC2100 series Gates	(22 mA) (12 mA)	-55°C to +125°C
MC2013 MC2063	1	(-2.5 mA)	9 5	MC2000 series Gates MC2000 series Gates	(22.5 mA) (12.5 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TI	EST CO	NDITIO	NS					
				mÅ							Volts				
(@ Test	ار)L	ار	ЭН		· v	v	W	V	v	1/	v	v	v
Ter	nperature	Pr*	Std	Pr*	Std	l _{in}	V _{IL}	VIH	V _R	V _{th 1}	¥th O	Vout	V _{cc}	V _{ссн}	V IHX
	(-55°C	22.0	12.0	-2.2	-1.2	1,0	0.45	2.7	4.5	2.0	0.9	5. 5	5.0	-	-
MC2113*, MC2163	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	(+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	
	(0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
MC2013*, MC2063	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	(+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

		Pin				2163 1				C2013							TEST CURI	RENT	/ VOLT	AGE A	PPLIED	TO P	INS LI	STED	BELOW	/ V :		1
		Under	_!	55°C	+:	25°C	-	25°C	_)°C	-	25°C	_	75°C		<u> </u>	T	Τ.	· 	1		T	т	1	1		r:	-
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	l ^{Or}	ОН	In	V _{IL}	VIH	V _R	V _{th 1}	V _{th O}	Vaut	Vcc	V _{CCH}	V _{IHX}	Gnd†
Input Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2,5	-	-2.5	mAdc	-	-	-	-	_	14	-	-	-	4	-	-	1,2,3,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-		-	1	-	-	-	4	-	-	2,3,10,14
Inverse Beta Current	IL	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Breakdown Voltage	BV _{in "0"}	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10
	BV _{in "1"}	1	5.5	-	5. 5	-	5.5	-	5. 5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,14
Output Output Voltage	v _{out ''0''}	13	-	0.45	-	0.45	-	0.45	_	0.45	-	0.45	-	0.45	Vdc	13	-	-	-	-	-	1	-	-	4	-	_	2,3,10
	Vout "1"	13	2.5	-	2.4	-	2,5	-	2.5	-	2.4	-	2.5	-	Vdc	-	13	-	-	-	-	-	1	-	4	-	-	2,3,10
Leakage Current	IOLK	13	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	13	4	-	-	1,2,3, 10,14
Short-Circuit Current	ISC	13	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10, 13,14
Output Voltage	V _{OL}	13	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	13	-	-	-	1	-	-	-	-	4	-		2,3,10
	V _{OH}	13	2.7	-	3.1	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	13	-	1	-	-	-	-	-	4	-	-	2,3,10
Power Requirements (Total Device) Maximum Power Supply Current	Imax	4	-	-	-	20	-	-		-	-	22	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3, 10,14
Power Supply Drain	IPDH	4	-	18	-	18	-	18	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	4		-	10‡
	I _{PDL}	4	-	12	-	12	-	12	-	15	-	15	-	15	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	ton	1, 13	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Turn-Off Delay	t _{off}	1, 13	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Rise Time	tr	1, 13	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Fall Time	t _f	1,13	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10

^{*} Prime Fan-Out

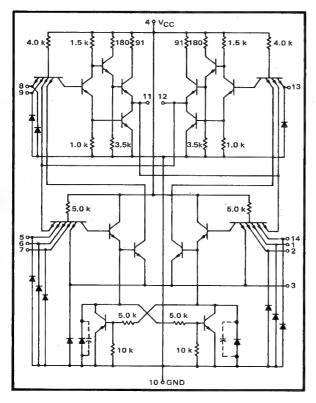
[†] Ground inputs to gates not under test during ALL tests unless otherwise noted.

The inputs to all gates must be ungrounded.

MTTL II MC2100/2000 series

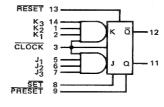
"AND" J'K FLIP-FLOP

MC2109 · MC2159 MC2009 · MC2059



The MC2009, MC2059, MC2109, and MC2159 are clocked flip-flops that trigger on the negative edge and perform the J-K logic junction. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gates in counters and certain other applications. A direct SET, PRESET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in a high state. When the clock returns low, the information is transferred to the bistable section and the Q and $\overline{\mathbf{Q}}$ outputs respond accordingly. The information on the J and K,inputs should not be changed while the clock is high. Each flip-flop can be set or reset directly by the direct $\overline{\mathbf{SET}}$, $\overline{\mathbf{PRESET}}$, or $\overline{\mathbf{RESET}}$ inputs. Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



	EQUIVALENT CIRCUIT	
SET 8 0- 9 0- PRESET	11 12	o 13 RESET
J ₁ 5 0 J ₂ 6 0 J ₃ 7 0		14K ₃ 1 K ₂ 2 K ₁
V _{CC} = 4 GND = 10		CLOCK

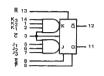
J	к	α_{n}	Q _{n+1}
. 0	0	0	0
0	0	-1	1
0 0 0	1	0	0
0	1	1	0
1	0	0	1
1	0	1 1	1
1	1	0	1
1 ,	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$ $K = K_1 \cdot K_2 \cdot K_3$

Total Power Dissipation = 40 mW typ/Pkg Switching Times: ton = 20 ns typ toff = 13 ns typ

SERIES	INPUT L FAC	OADING TOR	(1	F)	OUTPUT DRIVE	(1)	TEMPERATURE
SETTLES	CLOCK	ALL OTHER	CLOCK	ALL OTHER		(I _{OL})	RANGE
MC2109 MC2159	1.00	0.66	(-2.0 mA)	(-1.33 mA)	11 MC2100 series Gates 6 MC2100 series Gates		-55°C to +125°C
MC2009 MC2059	1.00	0.66	(-2.5 mA)	(-1.66 mA)	9 MC2000 series Gates 5 MC2000 series Gates		0°C to +75°C

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



								TES	t coni	DITIONS				
				m/	1					٧	olts			
	@ Test	ار)L	10	ЭН		21	V	v	v	v	v	v	V _{cc}
Ten	nperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	V _{IL}	ViH	V _R	V _{th 0}	V _{th 1}	out	*cc
	(−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0
MC2109*, MC2159	₹ +25°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	+125℃	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0
	0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0, 45	3.0	4, 5	1,1	1.9	5.5	5.0
WC2009*, MC2059	} +25°C	22. 5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4. 5	1.2	1.8	5.5	5.0
	(+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5 5.5 5.5	5, 0

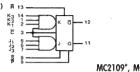
Pin MC2109, MC2159 Test Lim Under −55°C +25°C +125°							2009,							TEST CU	RRENT	/ VOL	TAGE	APPLI	ED TO PINS	LISTED	BELOW	l:					
Characteristic	Symbol	Under Test						25°C Max	Min			5°C May		75°C	Unit	lou	Гон	l _{in}	2 I _{in}		V _{IH}	V _R	V _{th 0}			V _{cc}	Gnd
input Forward Current	I _F	1		-1.33		-1.33		-1.33		-1.66		-1.66			6 mAdo		-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	-	4	1,8,10
		5	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-		5,10,13
		8	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
		9	-		-		-		-		-	ļ	-			-	-	-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-		9,10,13
		13	-	•	-		-		-	,	-	 	-	↓	•	-	_	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-	+	8,10,13
Leakage Current	I _R	1 5 8 9	-	100		100	-	100		100	-	100		100	μAdd		-	-	-	-	1 1 1 2	1 5 8	-	-	-	4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14 1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14
		13	-	+	-	*	-	*		+	-	+	-	+	+	-	-	-	-		-	13		-	-	+	1,2,3,5,6,7,10,11,14
Inverse Beta Current	· I _L	1 5 8 9 13	-	100		100	-	100		100	-	100	-	100	μAdd	- - - -	-	-	-	8 13	-	1 5 8 9 13	-	-	-	4	10
Breakdown Voltage	BV _{in"0"}	1 5 8 9	5.5	-	5.5		5.5	11111	5.5	11111	5.5	7	5.5	-	Vdc	- - -		1 5 8 9	-	8 13 ↓	-	-	-	-	-	4	10
	BV _{in"1"}	1 	5.5		5.5		5.5	1 1 1 1	5.5	-	5. 5		5.5	-	Vdc		-	1 5 8 9 13	-	-	-			-	-	4	2,3,5,6,7,10,11,14 1,2,3,6,7,10,12,14 1,2,3,5,6,7,9,10,12,14 1,2,3,5,6,7,8,10,12,14 1,2,3,5,6,7,10,11,14

^{*} Prime Fan-Out.

(continued)

ELECTRICAL CHARACTERISTICS (continued) # 13 =

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	@	Test
Te	mp	eratu
	(-55
C2159	₹.	+25

						a.		TES	T COM	IDITIONS				
				m/	1					V	olts			
	@ Test	10	DL .	Ic	Н		21	v	V	V	v	V	v	v
en	nperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	٧	V _{iH}	V _R	Viho	V _{th 1}	V _{out}	V _{cc}
1	_55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2. 0	5.5	5.0
,	+25℃	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	+125℃	22.0	12.0	-1.5	-0.7	4.0	2.0	0.45	2.8	4, 5	0.9	1,4	5.5	5.0
	(0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0
•	+25℃	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0
	(+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0

MC2009*, N

NC:	20	59	3	4	-25
			(4	75
-	_			_	$\overline{}$

			_												,,,,	22.0	2, 2 0, 0	210	2.0	0, 10	0.0	1.0	4.4	1.1	0.0	0.0	
		Pin Under				2159 T 5°C		mits 25°C	MC O°	2009,		059 T 5°C		mits 5°C			TEST CUE	RENT	/ VOL	TAGE	APPLI	ED TO PINS I	LISTED	BELOW	<i>l</i> :		
Characteristic	Symbol	Test				Max									Unit	lou	I _{OH}	l _{in}	2 l _{in}	٧ _{sL}	V _{iH}	V _R	V _{th O}	V _{th 1}	V _{out}	V _{cc}	Gnd
Clock Input Forward Current	I _F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAde	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4	3,10
Leakage Current	IR	3	-	150		150	-	150	-	150	,	150	-	150	μAdc	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,10,14
Inverse Beta Current	I _L	3 3	-	200 200	-	200 200	-	200 200	-	200 200	-	200 200	-	200 200	μAdc μAdc		-	-	-	13 8	-	3 3	-	-	-	4	10 10
Breakdown Voltage	BV in ''0''	3 3	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	5.5 5.5	-	5. 5 5. 5	-	5.5 5.5	-	Vdc Vdc	-	-	-	3	13 8	-	-	-	-	-	4	10 10
	BV _{in"1"}	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-		3	-	-	-	-	-		4	1,2,5,6,7,10,14
Output Output Voltage	V _{out ''0''}	12 11 11	- 1 -	0.45		0.45		0.45		0.45		0.45		0.45	Vdc	12 11 11	- - -	-	-	- - -		-		13 9 8	-	4	3,8,10 3,10,13 3,10,13
	V _{out} "1"	12 11 11	2.5	- - -	2.4	1 1 1	2.7	- - -	2.5	- - -	2.4	1 1 1	2.5	1 1 1	Vdc	-	12 11 11		-	1 1 1		-	13 9 8	-		4	8,10 10,13 10,13
Leakage Current	IOLK	12 11	-	225 225	-	225 225	-	225 225		225 225	1 1	225 225	-	225 225	μAdc μAdc		-	-	-	-	-	-	-	=	12 11	4	1,2,3,5,6,7,8,9,10,13,14 1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	^I sc	12 11	-	-	-30 -30	-70 -70	-	-	-	-	-30 -30	-70 -70	-	-	mAdc mAdc		. 1		-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,12,13,14 1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V _{OL}	12 11 11	- - -	0.40	-	0.40	-	0. 45	-	0.40	1 1 1	0.40		0.45	Vdc ↓	12 11 11	-	1 1 1	-		13 9 8	 	-	-	-	4 ↓	3,8,10 3,10,13 3,10,13
	V _{ОН}	12 11 11	2.80	-	3. 20		3. 35 	-	3.00	-	3.10	-	3. 15	1 1 1	Vdc	-	12 11 11	- 1	1 1	13 9 8		-	1	-	-	4	8,10 10,13 10,13
Power Requirements (Total Device) Power Supply Drain	I _{PD}	4	-	12 12		12 12	-	1 2 12	-	14 14	-	14 14	-		mAde mAde	- - -	-		-	-	-	-	-	-	-	4	3,10,13 3,8,10
							$\overline{}$		-			ш.,					L								1	1	

^{*} Prime Fan-Out.

MC2109, MC2159/MC2009, MC2059 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 15 ns.

Provides direct SET, PRESET, and RESET inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

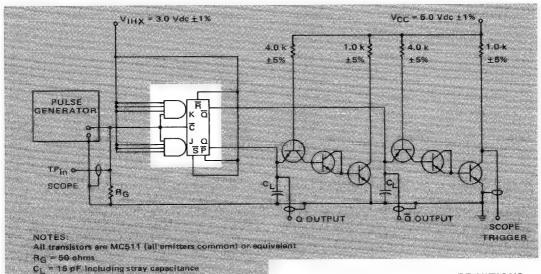
state to "0" state information change on the J and K terminals. The flip-flop will require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering — When the clock goes from

Negative edge triggering — When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Ω and $\overline{\Omega}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. $\overline{\text{PRESET}}$ and $\overline{\text{SET}}$ are tied to $\overline{\text{Q}}$; $\overline{\text{RESET}}$ is tied to $\overline{\text{Q}}$.

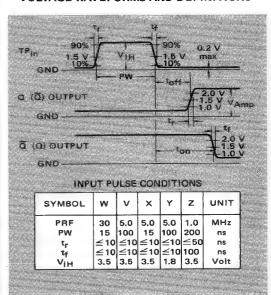
FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	мах	UNIT
Delay Time Off	toff	V	Sales.	20	ns
Delay Time On	ton	V		- 25	ns
Rise Time	4	l v		6.0	ns
Fall Time	¥	v		4.0	ris
Amplitude	Vamp	w E	3.2		Volt
(Device	WORST-C	ASE TEST with each		ulse)	
TEST	SYMBO	L CIMI	TS (INP CONDI	
Toggle Frequenc	Y Tog	30 MH	z max	VA.	1
Pulse Width	PW	15 ns n	nin	×	
Input High Volta	rge VIH	1.8 V i	nin,	Y	
Fall Time	t _e	100 ns	max	z	

VOLTAGE WAVEFORMS AND DEFINITIONS



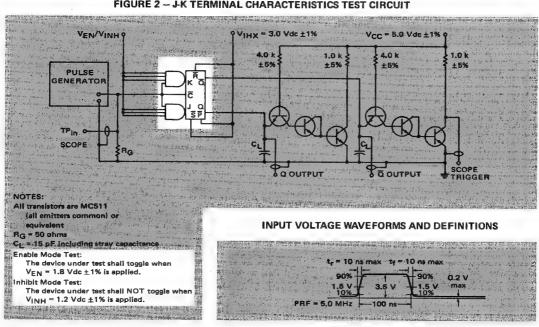
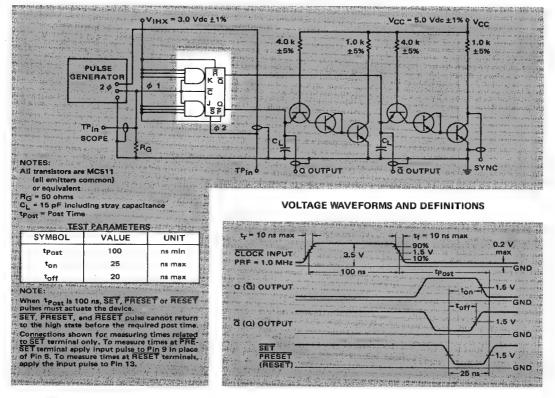


FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

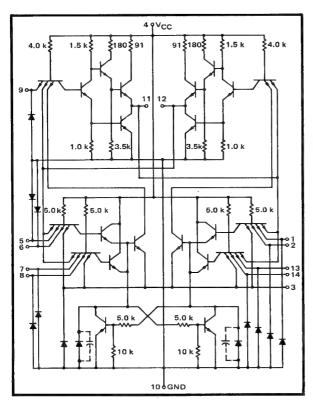




MTTL II MC2100/2000 series

"OR" J-K FLIP-FLOP

MC2110 · MC2160 MC2010 · MC2060

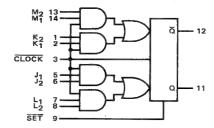


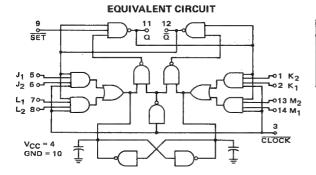
The MC2110, MC2160, MC2010, and MC2060 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct $\overline{\rm SET}$ is also available.

In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bistable section and the Ω and the $\overline{\Omega}$ outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct SET input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.

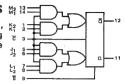




J	L	K	М	Q _n	Q _{n+1}	
0	0	×	×	0	0	X = Don't Care
1	×	l x	l x	0	1 1	Where J = J ₁ • J ₂ L = L ₁ • L
. × 1	1	×	×	0	1 1	L'= L ₁ • L
×	х	o	0	1	1 1	K = K ₁ • K
×	×	1	x	1	1 0 1	M = M1 • N
х	X	l x	1	1	0	

Total Power Dissipation = 50 mW typ/Pkg Switching Times: ton = 20 ns typ toff = 13 ns typ

SERIES	= . =	OADING TOR	(1	E)	OUTPUT DRIVE	(IOL)	TEMPERATURE
SENIES	CLOCK	ALL OTHER	CLOCK	ALL OTHER	OOTPOT BRIVE	(101)	RANGE
MC2110 MC2160	2.00	0.66	(-4.0 mA)	(-1.33 mA)	11 MC2100 series Gates 6 MC2100 series Gates		
MC2010 MC2060	2.00	0.66	(-5.0 mA)	(-1.66 mA)	9 MC2000 series Gates 5 MC2000 series Gates		0 ⁰ C to +75 ⁰ C



		L						1521	COND	LLION	5				
					mA							Volts			
	@ Test	I _c	N.	Ic	Н										
Ter	nperature	Pr*	Std	Pr*	Std	lin	2 I _{in}	4 I _{in}	V _{IL}	V _{iH}	V _R	V _{th 1}	V _{th O}	Vout	Vcc
	(−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
MC2110*, MC2160 -	+25°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	(+125°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
	(0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
MC2010*, MC2060	+25°C	22.5	12.5	-1.2	-0.6	1.0	2. 0	4.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	(+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

														<u> </u>	+75℃	22.5 12.5	-1.2 -0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0]
	1	Pin		MC2110	<u> </u>					AC2010	<u> </u>						TEST CUR	RENT	/ VOL	TAGE	APPL	IED TO	O PINS LIST	TED BE	LOW:			
cl	١, ,,	Under		55°C		25°C		25°C		°C		5°C		75℃			1 1	_							_	14	u	
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	JOI	ІОН	in	2 I _{in}	4 lin	V _{IL}	VIII	V _R	V _{sh 1}	Veho	V _{out}	Vcc	Gnd
Input Forward Current	$I_{\mathbf{F}}$	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAde	-	-	-	- ,	-	-	-	2,3,5,6,7, 8,13,14	-	-	-	4	1,9,10
		5	-		-		-		-		-		-			-	-	-	-	-	-	-	1,2,3,6,7, 8,13,14	-	-	-		5,10,11
		9	-	•	-	1	-	•	-	+	-	+	_	1	1	-	-	-	-	_	-	-	1,2,5,6,7, 8,13,14	-	-	-	1	3,9,10,11
Leakage Current	IR	1 5 9	-	100	-	100	- '	100	-	100	:	100	-	100	μAdc ↓	:	=	-	-	-	=	-	1 5 9	-	-	:	1	2,3,5,6,7,8,10,11,13,14 1,2,3,6,7,8,9,10,12,13,1 1,2,3,5,6,7,8,10,12,13,1
Inverse Beta Current	I _L	1 5 9	-	100	-	100	1 1 1,	100	1	100		100	-	100	μAdc	-	-	-	-	-	-	-	1 5 9	-	-	-	4	9,10 10,11 10,11
Breakdown Voltage	BV _{in "0"}	1 5 9	5. 5	-	5.5	-	5.5		5. 5	-	5.5	=	5. 5	:	Vdc	-	-	1 5 9	-	-	=	=	-	:	-	-	4	9,10 10,11 10,11
	BV _{in} "1"	1 5 9	5. 5	-	5.5	-	5. 5	-	5. 5	-	5.5	-	5. 5	Ē'	Vdc	-	-	1 5 9	-	-	:	=	-	-	-	=	4	2,3,5,6,7,8,10,11,13,1- 1,2,3,6,7,8,9,10,12,13,1 1,2,3,5,6,7,8,10,12,13,1
lock Input Forward Current	I _F	3	-	-4.0	-	-4.0	-	-4.0	-	-5.0	-	-5.0	-	-5.0	mAdc	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	4	3,10
Leakage Current	IR	3	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,8,10,13,14
înverse Béta Current	I _L	3	-	400 400	-	400 400	-	400 400	-	400 400	-	400 400	-	400 400	μAdc μAdc	-	-	- 1	-	-	:	-	3	:	:	-	4 4	9,10 10,11
	BV _{in ''0''}	3 3	5.5 5.5	-	5, 5 5, 5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	5.5 5.5	-	Vdc Vdc	-	-	-	-	3	-	-	-	-	-	= ,	4	10, 11 10, 12
	вv _{in ''1''}	3	5.5	<u> </u>	5.5	-	5, 5	-	5.5		5, 5	-	5. 5	-	Vdc	-	-	-	3	-	-	-	-	-	-	-	4	1,2,5,6,7,8,10,13,14
Output (For Set Only) Output Voltage	v _{out ''0"}	11	-	0, 45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11①	-	-	-	-	-	-	-	9	-	-	4	3, 10
	V _{out} "1"	11	2,5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-		,-	-	-	-	-	9	-	4	3,10
Leakage Current	IOLK	12 11	-	650 650	-	650 650	-	650 650	-	650 650	-	650 650	-	650 650	μAdc μ Ad c	-	-	-		-	-	-	12 11	-	-	-	4	1,2,3,5,6,7,8,10,11,13,1 1,2,3,5,6,7,8,9,10,13,1
Short-Circuit Current	I _{SC}	12 11	-	-	-30 -30	-70 -70	-	-	-	-	-30 -30	-70 -70	-	-	mAdc mAdc	-	= -	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,10,11,12,13 1,2,3,5,6,7,8,9,10,11,13
Output Voltage	v _{он}	12 11	2.80 2.80	-	3.20 3.20	-	3.35 3.35	-	3.00 3.00	-	3, 10 3, 10	-	3. 15 3. 15	-	Vdc Vdc	-	12 11	-		-	-	-	-	-	-	-	4	3,10,11 3,10,12
	VOL	12 11	-	0.40 0.40	-	0.40 0.40	-	0. 45 0. 45	-	0.40 0.40	-	0.40 0.40	-	0.45 0.45	Vdc Vdc	12① 11①		-	-	-	-	9	-	-	-	-	4	3,10 3,10
Breakdown Voltage	Io	12 11	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	-	4.25 4.25	mAdc mAdc	-	-	-	-	-	-	-	-	-	-	12 11	4	1,2,3,5,6,7,8,10,11,13,1 1,2,3,5,6,7,8,9,10,13,1
Power Requirements (Total Device)	I	4	_	15	_	15	_	15		18	_	18	_	18	Vdc				_				_		_		4	3,10,12
Power Supply Drain	I _{PD}	4	-	15	-	15	-	15	-	18	-	18	-	18	Vdc	-	-	-	-	_	-	-	-	_	-	-	4	3,10,11

MC2110, MC2160/MC2010, MC2060 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 15 ns.

The application of a "0" state to the $\overline{\text{SET}}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering — When the clock goes from the high state, the information in the temporary storage section is transferred; and the Q and \overline{Q} outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

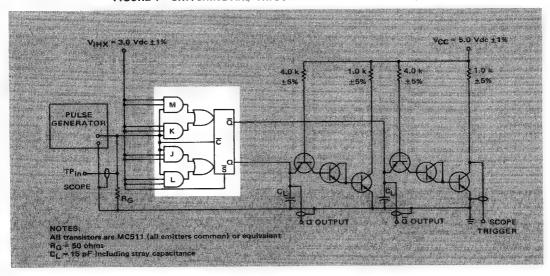
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

If both J, K, L, or $\ensuremath{\mathbb{M}}$ inputs are unused, they MUST be tied to ground.

Unused \overline{SET} is tied to $\overline{\Omega}$.

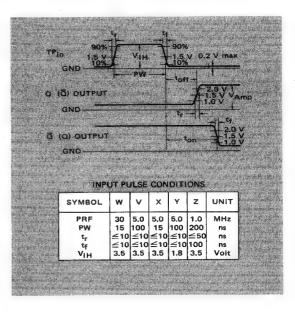
FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS

SWITCHING TIMES

TEST	TEST SYMBOL	PULSE	MIN	MAX	UNIT
Delay Time Off	Loff	V		20	ns
Delay Time On	ton	Y		25	ns
Risa Time	4	V =		6.0	198
Fall Time	T.	.		4.0	ms
Amplitude	VAmp	٧	3.2		Volt
(Clevice	WORST-Community toggle			ulse)	
TEST	SYMBO	LiMi	TS 🗆	INP CONDI	
Toggle Frequent	y frog	30 MH	z mex	٧	1
Pulse Width	. PW	15 ns n	nin		•
Input High Volt	age VIH	1.8 V n	nin		6.4
Fall Time	i te	100 ns	max	19	ery tra



MC2110, MC2160/MC2010, MC2060 (continued)

FIGURE 2 — J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT

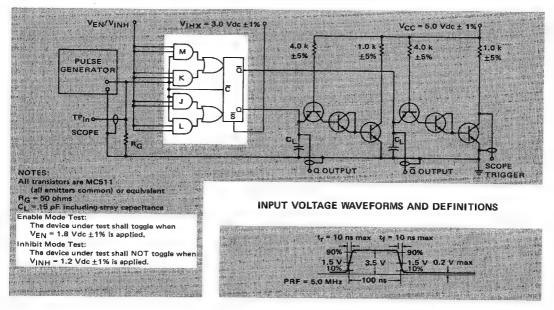
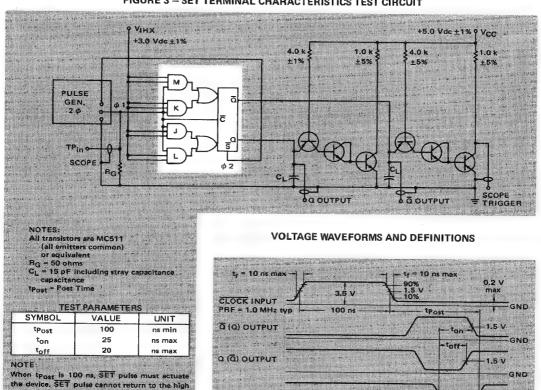


FIGURE 3 - SET TERMINAL CHARACTERISTICS TEST CIRCUIT



SET INPUT

1.5 V

- 25 ns

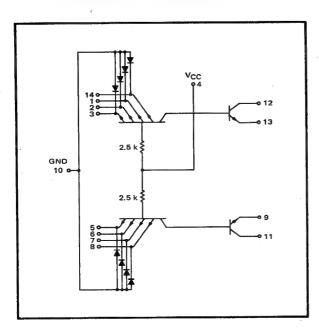
GND

state before the required post time.

DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL II MC2100/2000 series

MC2106 · MC2156 MC2006 · MC2056



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC2102 series and the MC2106 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 14 mW typ/Pkg.

Propagation Delay Times:

Δtpd = +1.0 ns typ
When added to the expandable

AND-OR-INVERT gates.

Δt_{pd}/pF = +0.7 ns/pF typ

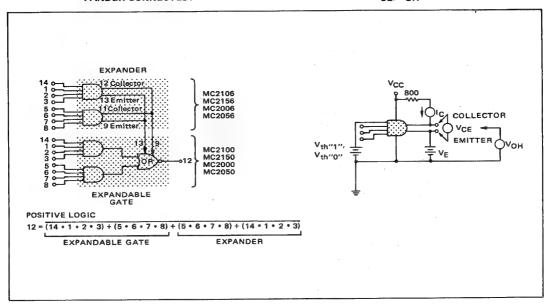
Caused by additional capacitance
at expansion points.

SERIES	INPUT LOADING FACTOR	(IE)	TEMPERATURE RANGE
MC2106 MC2156	1	-2.0 mA	-55°C to +125°C
MC2006 MC2056	1	-2.5 mA	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EX-PANDER CONNECTED.

VCE, VOH TEST CIRCUIT



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.

	Collector
14	
	Emitter
	Emitter
5 7 8	
	Collector

							TEST	CON	DITION	VS.					
(@ Test	n	ıΑ		-				Vol	s					
Ter	Temperature I _C I _{in} V _R V _{E1} V _{E2} V _{E3} V _{th 1} V _{th 0} V _{out} V _{CR} V _{CRH} V _{CC} V _{CCH} V _{CCH} V _{CC} V _{CC} V _{CCH} V _{CC} V _{CCH} V _{CC} V _{CC}														
	(−55°C	6.0	1.0	4.5	1.00	0.90	0.8	2.0	0.9	5.5	*	-	5.0	-	
MC2106, MC2156	₹ +25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.7	1.1	5.5	*	**	5.0	8.0	
	(+125℃	6.0	1.0	4.5	0.65	0.55	0.8	.1.4	0.9	5.5	*	-	5.0	-	
	(0°C	6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5,5	*	-	5.0	-	
MC2006, MC2056	{ +25℃	6.0	1.0	4.5	0.85	0.75	0.8	1.8	1.1	5.5	*	**	5.0	7.0	
•	(+75°C	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	* -	-	5.0	-	

														(173 C	10.0	1 4.0	1.0	10.15	0.00	V. 0	1. 1	1.0	0.0	7	- 1	5.0	-	1
		Pin.	MC	2106,	MC2	156 Te	st Lin	nits	MC	2006,	MC2	056 T	est Li	mits			7	ECT C	IDDEN	7 / 1/0	UTAC!		HIED 1	CO DIN	C LICT	PD DEI	014	1	
		Under	-5	5°C		25°C		25°C	. ()°C	+:	25°C	+7	′5°C	1	40.7	1			_						ED BEL	UW:		
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	l _c	l _{in}	VR	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th 0}	Vout	V _{CR}	VCRH	Vcc	V _{CCH}	Gnd†
Input											Γ	Π					1						T				<u> </u>	 	-
Forward Current	$I_{ m F}$	1		-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAde	-		2,3,14	-	-	-	-	-	-	- :	-	4	-	1,10
Leakage Current	I_{R}	1		100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1		-		-	1-		-	-	4	-	2,3,10,14
Inverse Beta Current	I_{L}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	12	-	4	-	10 .
Breakdown Voltage	BV in ''0''	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	12	-	4	-	10
	BV _{in''1''}	1	5.5	-	5.5	-	5.5	´-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Output																													
Output Voltage	· VOH	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	13	-	-	1	-	12	_	4	-	10
	v _{CE} ①	12	-	0.65	-	0.65	-	0.65	_	0, 65	-	0.65	-	0.65	Vdc	12	-	-	13	-	-	1	-	-	-	-	4	-	10
Leakage Current	IOLK	12	-	250	-	250	-	250	-	250	-	250	-	250	μAde	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14
Power Requirements																													~
(Total Device) Maximum Power Supply Current	I _{max} ②	4	-	-	-	7.0	-	-	7-	-	-	7.5	-	-	mAdc	-	-	-	-,	-	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,14
Power Supply Drain	IPDH	4	-	3.0	-	3.0	-	3.0	-	3.6	-	3.6	-	3.6	mAdc	-	-	-	-	-	9,13		-	-		-	4	-	10‡
	I _{PDL}	4	-	4. 25	-	4. 25	-	4. 25	-	5. 25	-	5. 25	-	5. 25	mAdc	-		-		-	- ;	-51	_	`	-	-	4	-	1,2,3,10,14

^{*} Indicated pins tied to $V_{\mbox{\footnotesize CC}}$ thru $\,$ 800 ohms $\,\pm\,1.0\%$ resistor.

^{**} Indicated pins tied to V_{CCH} thru 800 ohms \pm 1.0% resistor.

[†] Ground inputs to gate not under test during ALL tests, unless otherwise noted.

[#] The inputs of both gates must be ungrounded.

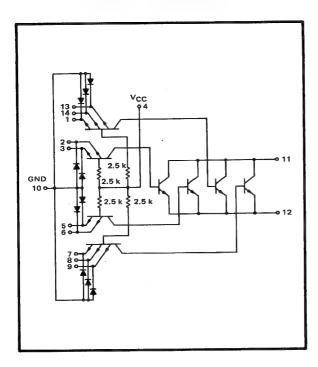
① VCE is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

² Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

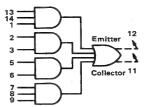
4-WIDE 3-2-2-3 INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL II MC2100/2000 series

MC2102 · MC2152 MC2002 · MC2052



This device consists of two 2-input and two 3-input AND gates ORed together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC2102 series or the MC2106 series expander package.



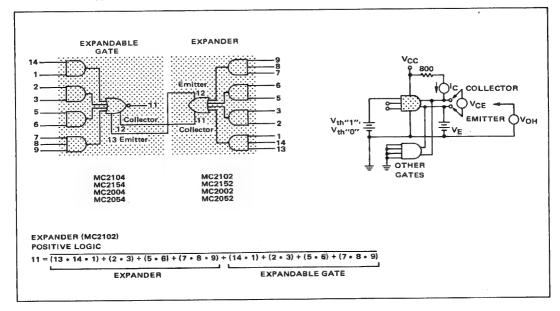
Total Power Dissipation = 28 mW typ/Pkg. Propagation Delay Times: $\Delta \tau_{pd} = +2.0 \text{ ns typ}$ When added to the expandable AND-OR-INVERT gates. $\Delta \tau_{pd}/pF = +0.7 \text{ ns/pF typ}$ Caused by additional capacitance at expansion points.

SERIES	INPUT LOADIN FACTOI		TEMPERATURE RANGE
MC2102 MC2152	1	-2,0 mA	-55°C to +125°C
MC2002 MC2052	1	-2.5 mA	0°C to +75°C

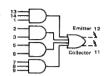
Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT"
GATE WITH A 4-WIDE 3-2-2-3 INPUT EXPANDER CONNECTED.

VCE, VOH TEST CIRCUIT



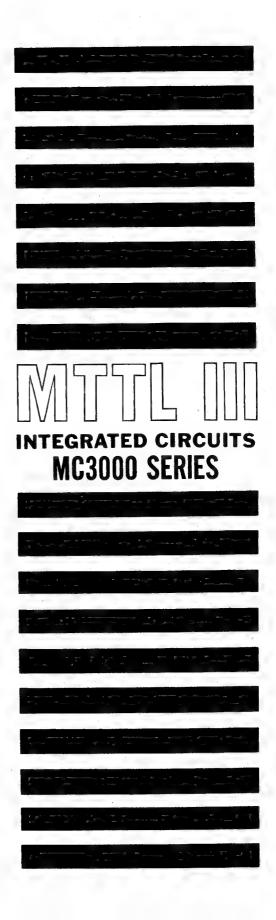
Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



						. 1	EST C	ONDIT	IONS		,			
	@ Test	m	A						Volts					
	emperature	lc	l _{in}	V _R	VEI	V _{E2}	V _{E3}	V _{th 1}	V _{th 0}	Vout	V _{CR}	V _{CRH}	V _{cc}	V _{CCH}
	_55°C	6.0	1.0	4.5	1.00	0. 90	0.8	2.0	0.9	5.5	*	-	5.0	-
MC2102 , MC215	2 } +25℃	6.0	1.0	4.5	0.85	0.75	0.8	1.7	1.1	5.5	*	**	5.0	8.0
	(+125℃	6.0	1.0	4.5	0.65	0. 55	0.8	1.4	0.9	5.5	*	-	5.0	-
	(0℃	6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5.5	*	-	5.0	-
MC2002 , MC205	2	6.0	1.0	4.5	0.85	0.75	0,8	1.8	1.1	5.5	*	**	5.0	7.0
	(+75℃	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-

														- (+75℃	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-	1
		Pin Under		C2102 55°C		2152 1 25°C	_					052 T					1	EST CURR	ENT /	VOLT	AGE A	PPLIE	о то	PINS I	ISTED	BELOW	1:		
Characteristic	Symbol	Test						25°C Max		°C Max	Hin.	25°C Max	H)	75°C Max	Unit	I _c	l _{in}	V _R	V _{E1}	V _{E2}	V _{E3}	V.,	٧,,,	Vou	V _{CR}	V _{CRH}	Vec	V _{cch}	Gnd
Input Forward Current	I _F	1	-	-2.0		-2.0		-2.0	-	-2.5		-2.5		-2.5			-	2,3,5,6,7, 8,9,13,14		-	-	-	-	-	-	CKH	4	- ССН	1,10
Leakage Current	IR	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8, 9,10,13,14
Inverse Beta Current	I _L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAde	-	-	1	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV _{in"0"} BV _{in"1"}	1	5. 5 5. 5	-	5. 5 5. 5	-	5. 5 5. 5	- '	5. 5 5. 5	1	5.5 5.5	-	5.5 5.5	-	V dc V dc	-	1 1	-	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10 2,3,5,6,7,8,9,
Output																			-	-				-					10,13,14
Output Voltage	V _{CE} ①	11 11	4.8	0. 65	4.8	0.65	4.8	0.65	4.8	- 0.65	4.8	- 0.65	4.8	0, 65	Vdc Vdc	- 11	-	-	- 12	12	- -	- 1	1 -	-	11	-	4	-	2,3,5,6,7,8,9,10 2,3,5,6,7,8,9,10
Leakage Current	IOLK	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	1-	12	-	-	11	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	4	-	-	-	14	-	-	-	-	-	15	-	-	mAde	-	-	-	-	-	12	-	-	-	-	11	_	4	1,2,3,5,6,7,8, 9,10,13,14
Power Supply Drain	I _{PDH}	4	-	6.0	-	6.0	-	6.0	-	7. 2	-	7. 2	-	7.2	mAde	-	-	-	-	-	12	-	-	-	-	-	4	-	10
	IPDL	4		8.5	-	8.5	-	8.5	-	10.5	-	10.5	-	10.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,

^{*} Indicated pins tied to V_{CC} thru 800 ohms $\pm 1.0\%$ resistor. ** Indicated pins tied to V_{CCH} thru 800 ohms $\pm 1.0\%$ resistor. ① V_{CE} is referenced to the emitter Voltage (Pin 12).



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NUMERICAL INDEX (Functions and Characteristics)

 $V_{CC} = 5.0 \text{ V, } T_{\Delta} = 25^{\circ}\text{C}$

Function	Туре	Output Loading Factor Each Output	Propagation Delay ^t pd ns typ	Power Dissipation mW typ/pkg	Page No.
Quad 2-Input NAND Gate	MC3000	10	6.0	88	4-112
Quad 2-Input AND Gate	MC3001	10	9.0	112	4-110
Quad 2-Input NOR Gate	MC3002	10	6.0	122	4-114
Quad 2-Input OR Gate	MC3003	10	9.0	150	4-116
Friple 3-Input NAND Gate	MC3005	10	6.0	66	4-108
Dual 4-Input NAND Gate	MC3010	10	6.0	44	4-104
Single 8-Input NAND Gate	MC3015	10	8.0	22	4-102
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC3020	10	6.0	62.5	4-106
Dual 4-Input NAND Power Gate	MC3025	20	6.0	70	4-120
Dual 4-Input AND Power Gate	MC3026	20	9.0	90	4–118
Dual 3-Input 3-Output AND Series Terminated Line Driver	MC3028	*	9.0	56	4-124
Dual 3-Input 3-Output NAND Series Terminated Line Driver	MC3029	=	6.0	44	4-126
Dual 4-Input Expander for AND-OR-INVERT Gates	MC3030	**	***	15	4-122
AND J-K Flip-Flops	MC3050	10	f = 40 MHz	80	4-128
AND Input JJ-KK Flip-Flop	MC3052	10	f = 40 MHz	75	4-133
Dual Type Ď Flip-Flop	MC3060	10	f = 30 MHz	120	4–138
Dual J-K Flip-Flop	MC3061	10	f = 50 MHz	100	4-141
Dual J-K Flip-Flop	MC3062	10	f = 50 MHz	100	4-145

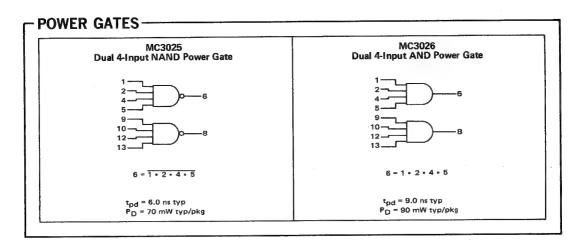
^{*}Direct Output = 10 minus the number of resistor-terminated outputs being used.

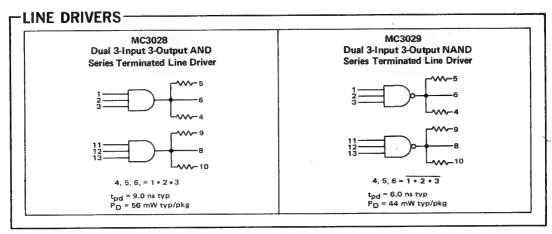
^{**}Full output loading factor of the expandable gate is maintained.

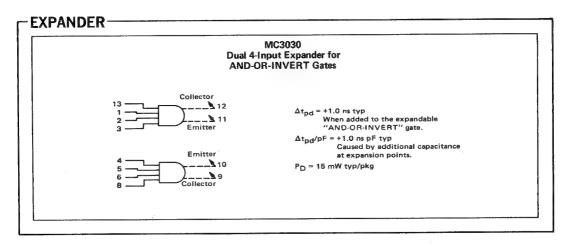
^{***} Δt_{pd} = +1.0 ns typ when added to the expandable AND-OR-INVERT Gate.

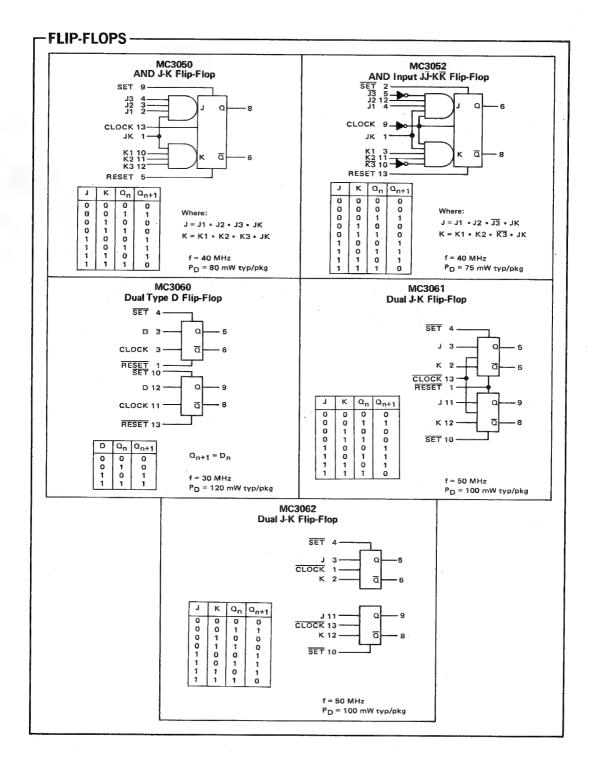
 $[\]Delta t_{pd}/pF = +1.0$ ns pF typ caused by additional capacitance at expansion points.

-GATES MC3000 MC3001 MC3002 Quad 2-Input NAND Gate **Quad 2-Input AND Gate** Quad 2-Input NOR Gate 10 12 12 13 13. 3=1+2 3 = 1 • 2 $3 = \overline{1 + 2}$ $t_{pd} = 6.0 \text{ ns typ}$ $P_D = 88 \text{ mW typ/pkg}$ t_{pd} = 9.0 ns typ $t_{pd} = 6.0 \text{ ns typ}$ $P_D = 122 \text{ mW typ/pkg}$ PD = 112 mW typ/pkg MC3003 MC3005 MC3010 Quad 2-Input OR Gate **Triple 3-Input NAND Gate Dual 4-Input NAND Gate** 10 12 13 3 = 1 + 212 = 1 • 2 • 13 6 = 1 • 2 • 4 • 5 t_{pd} = 9.0 ns typ P_D = 150 mW typ/pkg $t_{pd} = 6.0 \text{ ns typ}$ $P_D = 44 \text{ mW typ/pkg}$ $t_{pd} = 6.0 \text{ ns typ}$ $P_D = 66 \text{ mW typ/pkg}$ MC3015 MC3020 Single 8-Input NAND Gate Expandable Dual 2-Wide 2-Input **AND-OR-INVERT Gate** 10 Emitter 11 Collector 12 8 = 1 • 2 • 3 • 4 • 10 • 11 • 12 • 13 8 = (9 • 10) + (13 • 1) + (Expanders) $t_{pd} \approx 8.0 \text{ ns typ}$ $P_D = 22 \text{ mW typ/pkg}$ $t_{pd} = 6.0 \text{ ns typ}$ $P_D = 62.5 \text{ mW typ/pkg}$











GENERAL INFORMATION SECTION

INTRODUCTION

MTTL III integrated circuits are designed with speed approaching the limit for saturated logic and for good load driving capability. This line includes all the characteristics that have made transistor-transistor logic so popular. The major advantage of MTTL III over other TTL lines is the square transfer characteristic (Figure 1) that exists only for the MTTL III family. Because of this "ideal" transfer characteristic, the MTTL III family is the only TTL line that is truly compatible with MDTL. Another advantage of this family over competitive TTL lines is that it is designed to minimize problems associated with ringing.

The circuits in the MTTL III family are distinguished by a multiple-emitter input transistor, a darlington active "pull-up" in the upper output network, and an active bypass network in the base of the output pull-down transistor as shown in Figure 2.

The multiple-emitter input configuration offers the maximum logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The

Darlington output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allows high-speed operation while driving large capacitive loads.

The active bypass shown in the dotted area of Figure 2 holds the phase inverter transistor "off" until gate threshold is reached. This circuit operation provides the squared transfer characteristic shown in Figure 1.

In addition to improving the transfer characteristic, the bypass network offers a number of advantages compared to a simple resistor that can be traced to a much smaller impedance variation with temperature.

- Lower bypass impedance for the reverse current of the output transistor at elevated temperatures, provides faster turn-off.
- A lower current spike during the turn-off transient causes a lower ac power factor resulting in a lower total power consumption. This advantage is even more pronounced at higher temperatures.
- 3. Faster turn-on at low temperature.

FIGURE 1 — COMPARISON OF CONVENTIONAL TRANSISTOR-TRANSISTOR LOGIC AND MTTL III

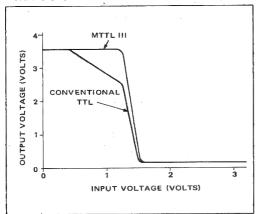
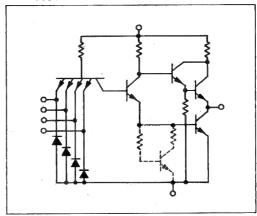


FIGURE 2 - TYPICAL MTTL III CIRCUIT





GENERAL INFORMATION SECTION

TYPICAL CHARACTERISTICS

Typical operating characteristics of the MTTL III family include: (Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.)

Supply Voltage Operating Range = 4.5 to 5.5 volts.

Operating Temperature Range: MC3000 Series 0 to +75°C

Output Drive Capability

Gates (Output Loading Factor) MC3000 Series = 10 Gates:

Capacitance = 600 pF

Output Impedance

High State = 10 ohms nominal (unsaturated)

Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits

#5.5 volts maximum

-1.5 volts minimum (4)

Switching Threshold = 1.5 volts nominal

laput Impedance

High State = 400 k ohms nominal

Low State = 2.4 k ohms nominal

Worst-Case de Noise Margin

High State = 0.700 volt minimum

Low State = 0.700 volt minimum

Power Dissipation

22 mW per gate typical 50-80 mW per flip flop typical

Average Propagation Delay - 6.0 ns per gate typical

13 ns per flip-flop typical

Rise Time = 1.0 ns typical

Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC3061) = 50 MHz maximum.

- (1) Assuming unused inputs are returned to voltage not greater than 4.0 Vdc.
- (2) The switching characteristics of the MTTL III family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turnoff delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2}$$
 ns

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative output transition from the 2.0 V to the 1.0 V level.

"NAND" GATES

The basic gate of the MTTL III logic family is the positive logic NAND gate. This gate is characterized by high speed, good load driving capability, superior transfer characteristic, and freedom from ringing problems. Representative of the various NAND gates presently available in the MTTL III family is the 4-input NAND gate (1/2 of the MC3010) shown in Figure 3.

"AND" GATES

While it is possible to design a complete logic system with NAND logic, it is often desirable to use other logic forms to save circuits, power dissipation, and propagation delay. Therefore, the positive logic AND function has been added to the MTTL III family.

Examples of the AND function are the standard quad 2-input gate, dual 4-input gate, dual 4-input power gate and a dual 3-input, 3-output line driver.

The technique used to form the AND function is the addition of an inverter to the basic NAND circuit. As shown in Figure 4, the inverter transistor with a collector resistor and an offset diode connected to its emitter is inserted between the multiple-emitter input transistor and the basic circuit phase-splitter transistor. The extra inversion adds only 3.0 ns propagation delay and about 6.0 mW additional power dissipation.

FIGURE 3 - MTTL III POSITIVE LOGIC "NAND" GATE CIRCUIT

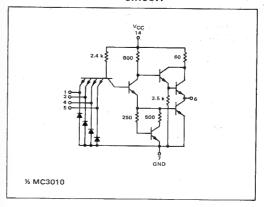
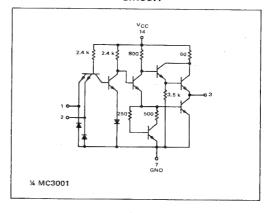


FIGURE 4 - MTTL III POSITIVE LOGIC "AND" GATE CIRCUIT





GENERAL INFORMATION SECTION

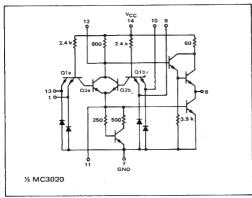
"AND-OR-INVERT" GATES

Unlike the MDTL family of logic circuits, the outputs of MTTL logic circuits cannot be tied together to perform the "Implied AND", often called the "Wired OR" function. If the outputs of the MTTL family devices are tied together, the lower output transistor of one circuit and the upper output transistor of another circuit can be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground, and due to excessive current flow, the saturated output state cannot be maintained and the desired logic function is not satisfied.

To retain the logical advantages offered by the "Implied AND" with the speed and load driving capability of an active pulp, the MTTL III family offers an AND-OR-INVERT Gate. The gate in Figure 5 incorporates two 2-input AND functions with outputs that are ORed and inverted. The AND function is provided by two multiple-emitter input transistors (Q1a and Q1b). The OR and INVERT operation is accomplished by two paralleled transistors (Q2a and Q2b) sharing a single collector resistor and a single bypass network. These paralleled transistors in turn drive the standard output.

The common collector and emitter nodes of one gate in each package are available externally to permit expansion.

FIGURE 5 - MTTL III "AND-OR-INVERT" GATE CIRCUIT



EXPANDER AND EXPANDER NODES

The ORing nodes of ½ the MC3020 dual AND-OR-INVERT Gate (Figure 5) are available for expanding the number of AND gates to four. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded, The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

"NOR" GATES

To save inverters, the system designer often needs the positive logic NOR function as well as the negative logic NOR available with the standard NAND gate. This capability is incorporated in the MTTL III line in the form of the MC3002, quad 2-input NOR Gate. The NOR gate is a modified AND-OR-INVERT gate with only a single emitter on each input transistor, as shown in Figure 6.

"OR" GATES

To provide the system designer with still another tool for optimum design, the MTTL III Series also offers the positive logic OR function. As shown in Figure 7, the OR is essentially a NOR gate with an additional inverter.

POWER GATES

Standard MTTL III gates offer good load driving capability and high fan-out. In most systems, however, there are a few applications that exceed the capability of a standard gate. The MTTL III power gates, shown in Figure 8, are designed to meet these requirements with a minimum of additional circuitry. Available in both NAND and AND functions, the power gates feature output circuitry designed to provide twice the fan-out of conventional gates: 20 standard gate loads instead of 10.

FIGURE 6 – MTTL III POSITIVE LOGIC "NOR" GATE CIRCUIT

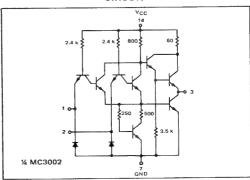
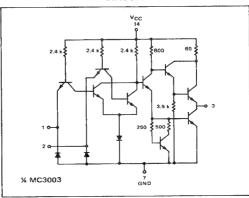


FIGURE 7 - MTTL III POSITIVE LOGIC "OR" GATE CIRCUIT



LINE DRIVERS

To minimize switching transients on long lines, the MTTL III family includes dual 3-input/3-output series-terminated line drivers. Two outputs have 75-ohm resistors in series with the standard output node, and one is connected directly to the node. A good match can be made at the output of each resistor when driving 93-ohm coax or 120-ohm twisted pair. For loads of 50 to 93 ohms, the two resistive outputs are paralleled for impedance matching. The non-resistive output can be used to drive adjacent loads in a normal fashion. The total number of output loads connected to the direct output (non-resistive output) is the standard fan-out of 10, minus the number of resistor terminated outputs being used.

Figure 9 shows 1/2 of the circuit of the MC3029, dual 3-input, 3-output series terminated NAND line driver. Figure 10 shows a typical application of this circuit and Figure 11 demonstrates the effects of series termination without a significant loss in high state noise immunity.

FIGURE 8 - MTTL III POWER GATE CIRCUIT (AND)

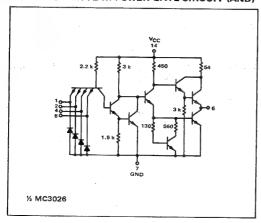
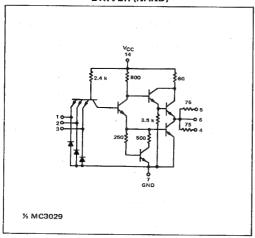


FIGURE 9 — MTTL III TERMINATED LINE DRIVER (NAND)



MTTL III

GENERAL INFORMATION SECTION

FIGURE 10 – TYPICAL APPLICATION OF THE LINE DRIVER

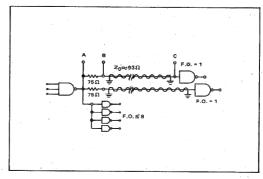
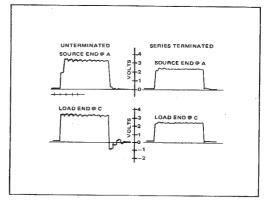


FIGURE 11 — EFFECTS OF SERIES TERMINATION WITH A MTTL III GATE DRIVING A 93-OHM LINE



OPERATING CHARACTERISTICS OF FLIP-FLOPS

The cornerstone of any modern logic family is the capability of its storage elements. The MTTL III flip-flops are designed to give maximum logic performance with fewer system restrictions than their predecessors. Three basic designs are typified by the MC3050, MC3060 and MC3061/MC3062. Common to all designs are:

1. Edge clocking.

The flip-flop is clocked at the normal MTTL III threshold voltage (approximately 1.5 V @ 25° C).

2. Overriding asynchronous inputs.

The direct SET and RESET inputs control the operation of the flip-flop regardless of the state of the clock or the information on synchronous inputs.



GENERAL INFORMATION SECTION

3. Short set-up times.

Prior to the clocking edge, the input information must become stable. The MTTL III flip-flops require only a minimum of time to read a "1" or a "0". Therefore data may be applied anytime in the clock period except during the time interval between the Set-up and Hold times. This characteristic permits higher clock frequencies or eliminates the necessity for critical control of clock pulse width.

 All inputs to the storage elements including the clock input have inputs that are compatible with all three MTTL families. The MC3050 and MC3060 flip-flops are positive edge triggered storage elements. That is, the inputs are enabled on the negative edge of the clock and the information is stored in the flip-flop on the positive edge of the clock. The MC3061 and MC3062 dual flip-flops are negative edge triggered devices and therefore operate in precisely the opposite manner. That is, data is stored on the negative edge of the clock.

In addition to the previously mentioned storage elements. The MC3052 Master-Slave flip-flop is also available. Data is stored in the Master flip-flop when the clock is low and transferred to the Slave flip-flop when the clock goes high.

Detailed discussion of each of the MTTL III flip-flops is provided on the individual data sheets.

FIGURE 12 – LOGIC DIAGRAMS OF EDGE-CLOCKED MTTL III FLIP-FLOPS

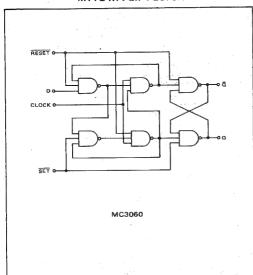
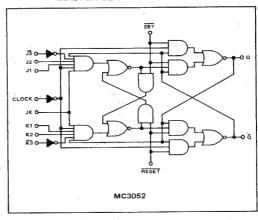
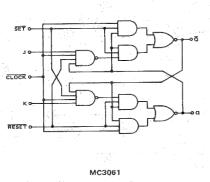
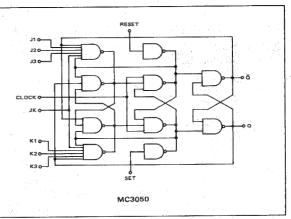


FIGURE 13 — LOGIC DIAGRAM OF MTTL III
MASTER-SLAVE J-K FLIP-FLOP







BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL circuit, the designer must always be aware of the problems caused by very high switching speeds. These switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the upper RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions will help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rates of change of current and voltage for a single MTTL III gate are in the range of $10^7~{\rm A/s}$ and $10^8~{\rm V/s}$ respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of $100~{\rm mils}$ or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL III circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every five packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The typical average dc power dissipation is given for each MTTL III device (3). It should be noted that the totem-pole output common to all high-level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.4 mW/MHz/output for a 15-pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL III circuits.

Unused Inputs and Unused Gates

To minimize potential problems resulting from external noise, the unused inputs of any MTTL III logic circuit should not be left open, but should either be tied to the used inputs or returned to a voltage between 2.0 and 5.5 Vdc. (For flip-flops, see appropriate data sheet for additional detail.) If the unused inputs are returned to a voltage, care should be exercised to insure that the absolute voltage between the most negative input level and that voltage does not exceed +5.5 volts. The total number of inputs that can be tied to the output of any driving gate is 25. (This is defined as high-state output loading factor.) It should be noted that the low-state output loading rules must still be maintained. The minimum logical "1" level for the high-state output loading is summarized for $V_{\rm CC} = 5.0$ V, $V_{\rm IL} = 1.1$ V, and $I_{\rm OH} = -2.0$ mA: $V_{\rm OH} = 2.5$ volts minimum @ 0°C.

To minimize power drain, the inputs of any unused gate in a package should be maintained at the level that would place the outputs in the high state (the low power dissipation state).

(3)
$$P_D = \frac{1}{1} \frac{$$

where IppL and IppH are the typical current drains at $V_{CC} = +5.0 \text{ V}$.

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage Continuous	+7.0	Vdc
Supply Operating Voltage Range	4.5 to 5.5	Vdc
Input Voltage	÷5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	0 to +75	ос
Storage Temperature Range — Flat Package	-65 to +175	°C
Plastic Package	-55 to +125	°C



GENERAL INFORMATION SECTION

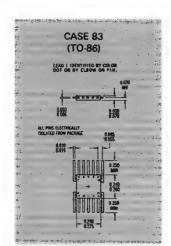
DEFINITIONS

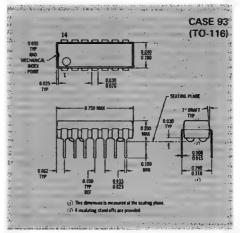
Poly at the second	months and a second	the state of the s
No.	8Vin	Input breakdown voltage
2	CT	Total parasitic especitance, which includes probe,
S		wiring, and load capacitances
Page 1	+c	Collector current
100	Ico	Expander collector leakage current
¥1.	in.	Input diode current with negative voltage applied
in .	1E	Emitter current
%	IEO	Expander emitter leekage current
iki .	EXE	Expander drive current at emitter node of AND-DR-
# C	EXE	INVERT gate
34.	1p	Input forward current with VCC applied
<u> </u>	1pg	Input forward current with VCCL applied
M	IF2	Input forward current with VCCH applied
No.	IFC	Clock Input forward current
£3"	1FD	D input forward current
ight.	IF1	J input forward current
48	IFK	'K input forward current
	FJK	JK input forward current
*****	IFR	RESET input forward current
São .	les	SET input forward current
ii.	lin	Input current
P.5-	l ₁₇₇₀₀₂₆	Maximum rated power supply current with V _{max}
tier .		applied
4	ЮН	Output high state current
die.	OHA	Unterminated output high state current
day .	OHB. C	Terminated output high state current
hr-	lou	Output low state current
\$10×	IOL1	Output low state current with VCCL applied
	OLIA	Unterminated output low state current with VCCL
ju i	OL.	applied
igo.	IQL2	Output low state current with VCCH applied
Gi.	IOL2A	Unterminated output low state current with VCCH
		applied
	OL18,10	Terminated output low state current with VCCL
i i i		applied
W.C.	IOL2A, 2C	Terminated output low state current with VCCH
Market 1		applied
	IPD	Flip-flop power supply drain current
# ·	PDH .	Power supply drain with inputs high
dir.	IPDL	Power supply drain with inputs low
ke. •	IR .	Input leakage current
# · ·	IRC"	Clock input leakage current
in.	RO	D input leakage current
Marie .	IRJ	J Input leakage current
3	IRK	K input leekage current
Barrello Bo	Marie with a finding	PROGRAMMENT OF THE PROGRAMMENT O

IRJK	JK input leakage current
IRR .	RESET input feakage current
IRS	SET input leskage current
Isc .	Short-circuit current
P1	Pulse used to set flip-flop state
PRF	Pulse repetition frequency
PW	Pulse width
ty	Fall time
*Hold "O"	Minimum time that low state data must be maintained
	after the clocking edge
"I" bloH [#]	Minimum time that high state datamust be maintained after the clocking edge
△tpd	Average increase in propagation delay per expander
pa	AND gate when connected to an AND-OR-INVERT
Atod/pF	Increesed propagation delay caused by additional
purv	capacitance at expansion points
tod "0"	Turn-on delay
tod "f"	Turn-off delay
tr	Rise time
fad "D"	Turn-on detay from asynchronous input
tert "1"	Turn-off delay from asynchronous input
	Minimum time that low state data must be applied
Set "0"	prior to the clocking edge
tSet "1"	Minimum time that high state data must be applied
	prior to the clocking edge
TPin	Test point at input of device under test
TPout	Test point at output of device under test
VBE mex	Emitter node threshold voltage for logic "0" output . level
VBE min	Emitter node threshold voltage for logic "1" output level
VCC	Power supply voltage
VCCH:	High power supply voltage
VCCL	Low power supply voltage
VD	Diode clamp voltage
VEET	Voltage applied to expender emitter for VOL test
VEE2	Voltage applied to expender emitter node for ICO
	test
VE	Maximum logic "0" level output voltage
VIH	Logic "1" threshold voltage
VIHX	Reduced supply voltage to hold input above three- hold and to prevent noise from entering the device
VIL	Logic "O" threshold voltage
	Maximum rated power supply voltage
Vmex	Output high voltage with IOH source current
VOH .	Output low voltage with IOL source current
VOL	Maximum output low voltage with VCCI applied
VOL1	Maximum output low voltage with VCCH applied
VOL2	Waxiums ontbut low voltage on terminated ontbut
VOL3	with V _{CCL} applied
VOL4	Maximum output low voltage on terminated output
	with VCCH applied
VR	Logic "1" minimum reverse voltage
VRH	Logic "1" meximum reverse voltage

PACKAGING

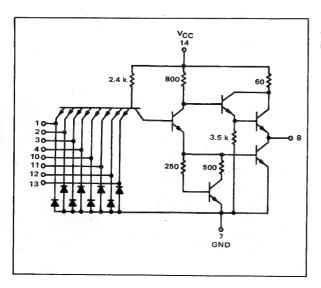
All MTTL III integrated circuits are available in the TO-85 14 lead flat package and TO-116 dual in-line plastic package. Suffix "F" to the basic type number; to order plastic package, add Suffix "P".



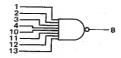


MTTL III MC3000 series

MC3015



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders and decoders.



Positive Logic:

8=1 • 2 • 3 • 4 • 10 • 11 • 12 • 13

Negative Logic:

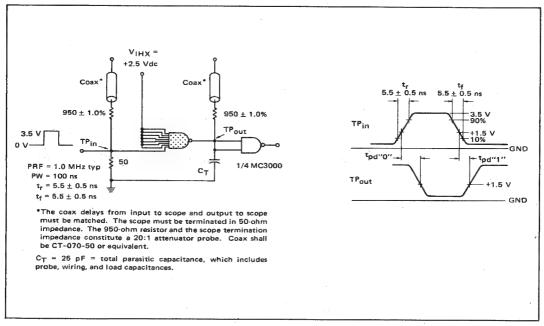
8 = 1 + 2 + 3 + 4 + 10 + 11 + 12 + 13

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 22 mW typ/pkg Propagation Delay Time = 8.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.

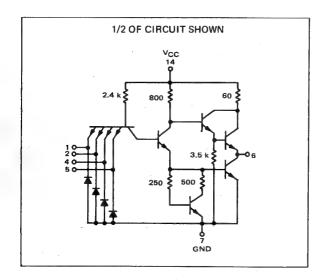


							TEST	CURR	ENT/VOLT	AGE VALUES	i				
@Test		r	nA							٧	olts				
perature	l _{OL1}	l _{OL2}	Іон	1 _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	V _{IHX}
0°C	19	23	-2.0		-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5, 5	_
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	19	23	-2.0		-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5	-

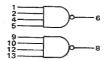
		Pin				est Limi								TEST	CURR	ENT / Y	/OLTA	GE APPLIE	TO PINS LI	STED BEL	OW:				
		Under	0,		_	5°C	+7.					Γ.	Τ.	,	u.		1/	, , , , , , , , , , , , , , , , , , ,	V	v	v	v	v	V	١ ا
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OL1	I _{OL2}	ІОН	in	1 _D	V _R	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	- 1	-	2, 3, 4, 10, 11, 12, 13	-	-		14	-	7
Leakage Current	IR	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-		14	-	2, 3, 4, 7, 10, 11, 12, 13
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-		-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13
Clamp Voltage	v _D	1	-	-	-	-1.5	1-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-,	14	-	-	7
Output Output Voltage	V _{OL1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	1	-	-	2, 3, 4, 10 11, 12, 13	-	-	14	-	-	7
	V _{OL 2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	1	-	-	2, 3, 4, 10 11, 12, 13	-	-	-	14	-	7
	v _{он}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	1	-	-	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7
Short-Circuit Current	I _{SC}	8	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-		-	-	14	-	-	-	1, 2, 3, 4, 7,8, 10, 11, 12,13
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	6.5	-	-	mAde	-	_	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Power Supply Drain	I _{PDH}	14	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 10, 11, 12, 13	-	14		-	-	7
	IPDL	· 14	-	4, 3	-	4.3	-	4.3	mAde	-	-		-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Switching Parameters	,									Pulse In	Pulse Out									2				2, 3, 4, 10,	
Turn-On Delay	t _{pd''0''}	1, 8	-	-	-	12	-	-	ns	1	. 8	-	-	-	-	· ,-		-	-	-	14			11, 12, 13	,
Turn-Off Delay	tpd"1"	1,8	-	-	-	12	-	-	ns	1	8	-	Γ-	-	-	-	-	-		-	14	-	-	2, 3, 4, 10, 11, 12, 13	7

MTTL III MC3000 series

MC3010



This device consists of two 4-input NAND gates. These gates may be cross-coupled to form a set-reset flip-flop.



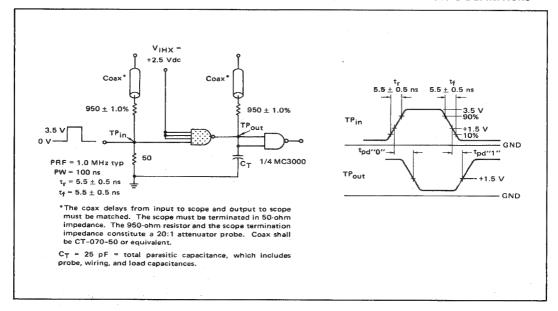
Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$ Negative Logic: 6 = 1 + 2 + 4 + 5

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 44 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TEST	CURR	ENT/VOLT	AGE VALUES					
@Test		n	nA							٧	olts				
Temperature	l _{ori}	l _{OL2}	I _{OH}	l _{in}	ΙD	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccl}	V _{CCH}	V _{IHX}
0°C	19	23	-2.0	-	-	1,1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5.5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0, 4	2.5	4.0	-	5.0	4.5	5.5	-

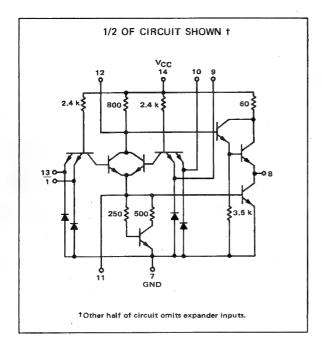
		Pin		MC	3010	Test Lim	its						•	TES	r Curi	RENT /	VOLTA	GE APPLIEI	D TO PINS LI	STED BEL	OW:	L	1 010		1
		Under	0	°C	+2	5°C	+7	5°C		-	Γ.	Π.	Τ.			-	_		1						
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OLI	I _{OL2}	Юн	lin	I _D	Vil	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	ν _{ccr}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAde	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	14	-	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	IR	1	-	80	-	80	-	80	μ Ad c	-	-	-	-	-	-	-	-	1	-	-	-		14	-	2, 4, 5, 7 *
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14		2, 4, 5, 7 *
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7
Output Output Voltage	V _{OL 1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V _{OL 2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	-	1	-	-	2, 4, 5	-	-	~	14	-	7*
	v _{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7*
Short-Circuit Current	I _{SC}	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	12. 5	~	-	mAde	-	-	-	-	-	-	-	-	-		14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I _{PDH}	14	-	18	-	18	-	18	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	IPDL	14	-	9.0	-	9.0	-	9.0	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters		1.0								Pulse In	Pulse Out										14			245	7*
Turn-On Delay	^E pd''0	1, 6	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	_	14	•	-	2, 4, 5	7*
Turn-Off Delay	tpd"1"	1, 6	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

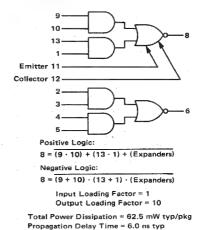
EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MTTL III MC3000 series

MC3020

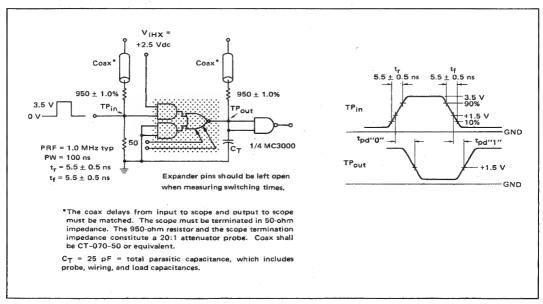


One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

TEST CURRENT/VOLTAGE VALUES Volts mA @Test VR VRH V_{max} V_{cc} V_{CCL} V_{CCH} V_{IHX} IOH Temperature l_{OL 1} 5. 5 2.5 4.0 5. 0 4.5 0°C 0.3 0.50 2.0 0.4 19 23 -2.0 5.0 4.5 5. 5 2.5 +25°C 19 23 -2.0 1.0 -10 0, 3 0.55 1.1 1.8 0.4 4.0 7.0 5.0 4.5 5. 5 0.70 0.9 1.8 0.4 4.0

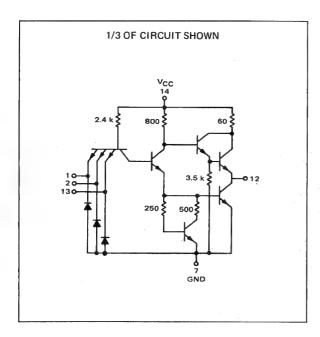
Symbol	Pin Under Test	MC3020 Test Limits																								
		0°C		+25°C		+75°C								1131	73111111	_					-	1,,		T.,	v	
		Min	Max	Min	Max	Min	Max	Unit	l _{OL1}	OL 2	loH	lin	وا	I _E	I _{EXE}	٧ _{ال}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	VCCL	VCCH	AIHX	x Gnd
I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	m A de	-	-	-	-	-	-		-	-	1	-	13	-	-	14	-	-	7,9,10*
I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-		-	-	-	1	-	13	_	-	-	14	-	7, 9, 10*
I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-		14	-	7, 9, 10, 13*
BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	14	-	7, 9, 10, 13*
v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1			-	-	-	-	-	-	-	14	-	-	7, 9, 10 *
V _{OL1}	8	-	0, 4 0, 4	-	0.4 0.4	-	0. 4 0. 4	Vdc Vdc	8	-	-	-	-	-	11, 12	-	1 -	-	-	13	-	=	14 14	-	:	7, 9, 10 * 1,7,9,10,13
V _{OL 2} V _{OL 2}	8	-	0. 4 0. 4	-	0. 4 0. 4	-	0.4	Vdc Vdc	-	8 8	-	-	-	-	11, 12	-	- 1	-	-	13	-	-	-	14 14	-	1,7,9,10,13* 7,9,10*
v _{он}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	-	-	1	-	-	-	13			14		-	1, 7, 10 *
^I SC	8	-	-	-30	-100	-	-	Vdc	-	-	-	-:	-	-	-	-	-	-	-	-		14	-	-		1, 7, 8, 9, 10, 13 *
V _{BE max}	- 11	-	1.010	-	0.975	-	0.935	Vde	8	-	-	-	-	-	11, 12			-	-	- -	-	-	14	-	-	1, 9, 10,
V _{BE min}	11	0.70	-	0.65	-	0,55	-	Vdc	-	-	-	-	-	11	-	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 12,13 *
I _{max}	14	-	-	-	24	-	-	mAdc	-	-		-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7 9,10,13
I _{PDH}	14	-	22	-	22	-	22	mAde	-	-	-	-	-	-		-	-	-	-	1, 2, 3, 4, 5, 9, 10, 13	-	14	-	-	-	7
I _{PDL}	14	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	~	14	-	-	-	1,2,3,4,5,7 9,10,13
t	1.8				12			ne	Pulse In	Pulse Out		-	_			_	_	_	_	_	_	14	-	_	13	7,9,10 *
-		-	_	-	12	Ë	 -	 	1	. 8	-	-	_	-	<u> </u>	-	 -	-	-	-	-	14	-	-	13	7, 9, 10 *
	IF1 IF2 IR BVin VD VOL1 VOL2 VOL2 VOH ISC VBE max VBE min Imax IpDH	Symbol Under Test IF1 1 IF2 1 BVin 1 VD 1 VOL1 8 VOL2 8 VOL2 8 VOL2 8 VOH 8 ISC 8 VBE max 11 VBE min 11 Imax 14 IpDH 14 IpDL 14 Ipd"o" 1,8	Symbol Under Test Min	Symbol Pin Under Test O°C IF1 1 - -1.9 IF2 1 - -2.3 IR 1 - 80 BVin 1 - - VD 1 - - VOL1 8 - 0.4 VOL2 8 - 0.4 VOL2 8 - 0.4 VOL 2 8 - 0.4 VOH 8 2.5 - ISC 8 - - VBE max 11 0.70 - Imax 14 - 22 IpDH 14 - 14 tpd"0" 1,8 - -	Print Under Test O°C +2 Min Max Min I _{F1} 1 1.9 - I _{F2} 1 2.3 - BV _{In} 1 80 - BV _{In} 1 5.5 - V _D 1 - VOL1 8 - 0.4 - VOL2 8 - 0.4 - VOL 2 8 - 0.4 - VOH 8 2.5 - 2.5 ISC 8 - 1.010 - VBE max 11 0.70 - 0.65 I _{max} 14 - 22 - I _{pd} ***** - 1.01 - I _{pd} ***** - 1.01 -	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Pin Under Test Min Max Min Max Min Max Min Home Min Max Min Home Min Max Min Home Min Max Min Home Min Min<	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Symbol Print Pri	$ \frac{V_{\text{phiholofformula}} V_{\text{phiholofformula}} V_{phiholofform$	$ \frac{V_{ymbol}}{V_{ymbol}} = \frac{V_{ymbol}}{V_$	$ \frac{1}{\text{Ny bol}} = \frac{1}{\text{Ny bol}} = \frac{1}{\text{Ny bol}} -\frac{1}{\text{Ny bol}} -\frac$	$ \frac{1}{Ny bod Power P$	

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test,

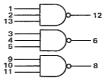
TRIPLE 3-INPUT "NAND" GATE

MTTL III MC3000 series

MC3005



This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



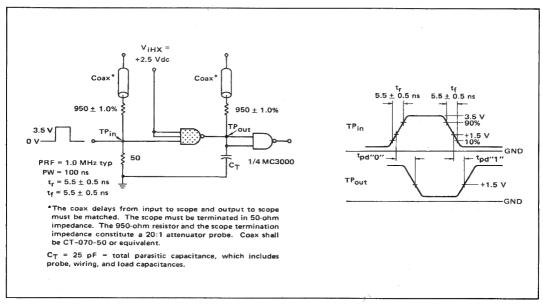
Positive Logic: $12 = 1 \cdot 2 \cdot 13$ Negative Logic: 12 = 1 + 2 + 13

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 66 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Test procedures are shown for only one agate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



							TEST	CURR	ENT/VOLT	AGE VALUE	S				
@Test			mA							٧	olts			-	
Temperature	lorı	l _{OL2}	IOH	l _{in}	l _D	٧ _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{mex}	V _{cc}	V _{ccl}	V _{CCH}	V _{IHX}
0°€	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5, 5	
+25°C	19	23	-2.0	1.0	-10	1, 1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	19	23	-2.0	-	•	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5	_

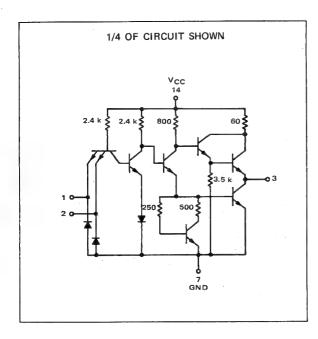
		Pin			3005	fest Lim	its					1		TEST	T CURI	PENT /	VOLTA	GE ADDITE	D TO PINS L	STED BEI	0.0	4.5	3. 3		1
		Under	0	°C	+2	5°C	+7	5°C		├──			_		_	_	_	T AT THE	D TO FINS L	ISTED BEI	LOW:				
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	lori	l _{O13}	IOH	lin	I _P	VIL	VIH	V _F	V_R	V _{RH}	V _{max}	Vcc	Vccl	V _{CCH}	VIHX	Gnd
input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2, 13	-	-	14	-	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	1	-	2, 13	-	-	-	14	-	7*
Leakage Current	I _R	1	-	80	-	80	-	80	μAde		-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 7, 13 *
Breakdown Voltage	BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-		-	-	-	-	14	-	2, 7, 13 *
Clamp Voltage	v _D	1		-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	+-	-	-	-	-	14	-		7*
Output Output Voltage	v _{OL1}	12	-	0.4	-	0.4	-	0.4	Vdc	12	-	-	-	-	-	1	-	-	2, 13	-	-	14	-	-	7*
	V _{OL2}	12	-	0.4	-	0.4	-	0.4	Vdc	-	12	-	-	-	-	1	-	-	2, 13	-	-	-	14	-	7*
	v _{OH}	12	2.5	-	2.5	-	2.5	-	Vdc	-	-	12	-	-	1	-	-	-	2, 13	-	-	14	-		7*
Short-Circuit Current	Isc	12	-	-	-30	-100	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 7,* 12, 13
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	20	-	-	mAde	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9, 10, 11, 13
Power Supply Drain	I _{PDH}	14	-	27	-	27	-	27	mAde	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 11, 13	-	14	-	-	-	7
	I _{PDL}	14	-	12.5	-	12.5	-	12.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5,7, 9,10,11,13
Switching Parameters	-								-	Pulse In	Pulse Out														0,10,11,10
Turn-On Delay	^t pd''0''	1, 12	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-		-	14	-		2, 13	7*
Turn-Off Delay	t _{pd"1"}	1, 12	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

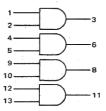
QUAD 2-INPUT "AND" GATE

MTTL III MC3000 series

MC3001



This device consists of four 2-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

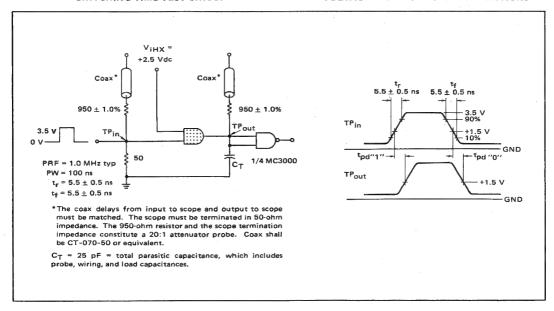


Positive Logic: 3 = 1 · 2 Negative Logic: 3 = 1 + 2

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 112 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT

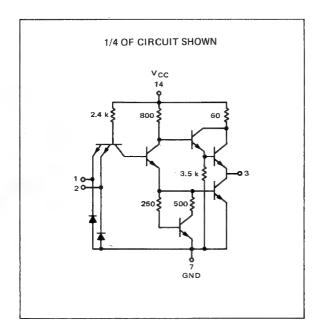


ELECTRICAL C	HARACT	ERISTI	CS	<u>'</u>	$\overline{}$	—з -			. [TEST	CURRENT/	VOLTAGE V	ALUES					
Test procedures ar				, 4	\preceq			<i>ര</i>	lest .		-	nA							Vo	lts					
ate. The other gate nanner. Further, tes				<u>-</u>	=	—-6		_	rature	l _{OL1}	l _{OL2}	I _{OH}	l _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	VIHX	
or only one input	of the gat	e under t	est, 1	"	_)-	8			0°C	19	23	-2.0	-		1.1	2, 0	0.4	2.5	4.0	-	5.0	4.5	5. 5	-	
Fo complete testing maining inputs.	g, sequence	e through	re- 1:	2		 11			+25℃	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5	-
			<u>'</u>						+75℃	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4, 5	5. 5		1
		Pin	0		3001 I	est Lim	+7	F°C		L				TEST	CURF	RENT / Y	VOLTA	GE APPLIED	TO PINS LI	STED BEL	.0W:				
Characteristic	Symbol	Under Test	Min	Max	Min	Max	Min	Max	Unit	lou	I _{OL2}	Гон	l _{in}	l _D	٧	V _{IH}	٧ _F	V _R	V _{RH}	$V_{\rm mex}$	V _{cc}	Vccr	V _{CCH}	VIHX	Gnd
Input												<u> </u>	-					ì							7
Forward Current	I _{F1}	1	· -	-1.9	-	-1.9	-	-1,9	· mAdc	-	-		-	-		-	1	-	2*	•	-	14	-		<u> </u>
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2*	-	-	-	14	-	7
Leakage Current	IR	1	-	80	-	80	-	80	μAdc	-		-	-	-	-	-	-	1	*	-	-	-	14	-	2,7
Breakdown Voltage	BVin	1	-	- 1	5. 5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,7
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc		-	-	-	1	-	-	-	-	*	- "	-	14	-	-	7
Output						<u> </u>			 				-		<u> </u>	1		<u> </u>							7
Output Voltage	V _{OL 1}	3		0.4		0.4	-	0.4	Vdc	3	-	-	-	_	1	-	-	-	2 *	-	_	14	-	-	
	V _{OL 2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3		-	-	1	-	-	~	2*	-	-	-	14	-	7
	V _{ОН}	3	2.5	-	2.5		2.5	-	Vdc	-	-	3	-	-	-	1	-		2*	-	-	14	-	-	7
Short-Circuit Current	Isc	3	-	-	-30	-100	-	-	mAde	-	-	-	-	-	-	-	-	2	1,2*	-	14	-	-	-	3,7
Power Requirements (Total Device) Maximum Power	Imax	14	-			34	-	_	m Adc	_	_	_	-		_	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-	-	7
Supply Current Power Supply Drain	IPDH	14	-	24	-	24	-	24	mAde	-		-	+-	-	-	+-	-	-	1,2,4,5,9,	-	14	-		-	7
		14	-	48	-	48		48	mAdc	-	-	-	 	-	_	+-	-	-	10,12,13	-	14	-	 -	-	1,2,4,5,7,
Switching	IPDL	**		30		10	<u> </u>	10	mzade	Pulse	Pulse		-	_	_	-	-	-	-		-	-	-		9,10,12,13
Parameters		1.2				19				In 1	Out 3		_	_	_			_	*	_	14	_	_	2	. 7
Turn-On Delay	pd''0"	1,3	-		-	12		-	ns			<u> </u>	ļ	ļ	ļ	ļ.	ļ.								
Turn-Off Delay	t pd''1''	1,3		-	-	12	-		ns	1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7

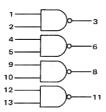
^{*}Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to $V_{\rm RH}$.

MTTL III MC3000 series

MC3000



This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

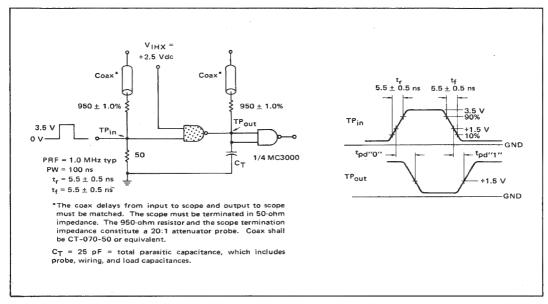


Positive Logic: $3 = \overline{1 \cdot 2}$ Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 88 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



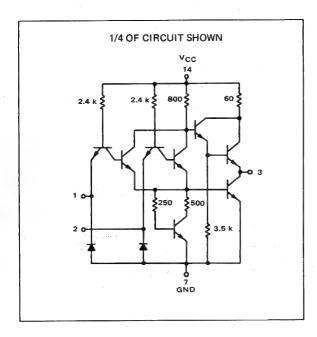
ELECTRICAL O	HARAC	TERIST	201	1		3																			
Test procedures a				4	\vdash							mA			7	1521	CURRE	NI / VULI	AGE VALUES	olts					-
gate. The other gate	es are teste	d in the	same	5	Ľ	6		_	Test erature	lou	I _{OL2}	I _{OH}	I _{in}	I _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{ccι}	V _{CCH}	V _{IHX}	1
for only one input				10	<u></u> _	8			0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4. 0	-	5. 0	4.5	5. 5	-	1 !
To complete testin maining inputs,	ig, sequend	ce throug		12)	11			+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5. 0	4.5	5. 5	2.5	
				14	20000	Test Lim	**		+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0		5.0	4.5	5.5		_
		Pin	_	°C		5°C	T	'5°C	T					TEST	CURR	ENT / \	/OLTA	GE APPLIEI	TO PINS LI	STED BEL	OW:				
Characteristic	Symbol	Under Test	Min	Max	Min	Max	Min	Max	Unit	I _{OL1}	I _{OL2}	I _{OH}	l _{in}	I _D	V _R	V _{IH}	V _F	V _R	V _{RH}	V _{mex}	Vcc	V _{ccl}	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	T .	-1.9	-	-1.9	-	-1.9	mAde		_	-			-	-	1	-	2	-	-	14	-	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2	-	-	-	14	-	7 *
Leakage Current	$I_{\mathbf{R}}$	1	-	80	-	80	-	80	μAde	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2,7 *
Breakdown Voltage	BVin	1	-	-	5.5	-		-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-		14		2,7*
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V _{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	<i>'</i> -	-	1	-	-	2	-	-	14	-	-	7*
	VOL 2	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	~	1	-	-	2	-	-	-	14	-	7*
	v _{ОН}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	1	-	-	-	2	-	-	14	-	-	7*
Short-Circuit Current	ISC	3	-	-	-30	-100	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	25	-	-	mAdc		-	-	-	-	-	-	-	-	-	14	-	-	-	· -	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I _{PDH}	14	-	36	-	36	-	36	m A dc	-	-	-	-	-	- :	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	IPDL	14	-	17.5	-	17, 5	-	17.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t _{od"0"}	1,3	_	_	_	10		_	ns	Pulse In	Pulse Out	_	_	-	_					_	14	_		2	7*
Turn-Off Delay	tpd"1"	1,3	-	-	-	10	-	-	ns	1	3	-	-	-	-	2	-	-	-	-	14	-	-	2	7*

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

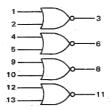
QUAD 2-INPUT "NOR" GATE

MTTL III MC3000 series

MC3002



This device consists of four 2-input NOR gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

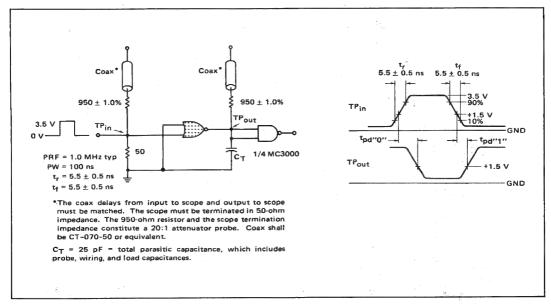


Positive Logic: $3 = \overline{1+2}$ Negative Logic: $3 = \overline{1+2}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 122 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. 10—To complete testing, sequence through re- 12—maining inputs.



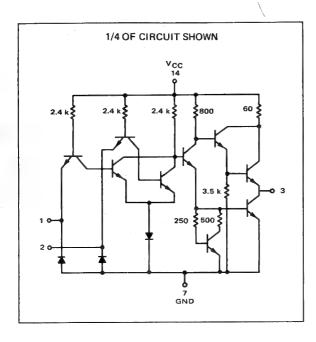
. [TEST	CURRI	NT/VOLTA	GE VALUES				
@Test		п	nA							V	olts			
Temperature	I _{OL1}	I _{OL2}	l _{ОН}	l _{in}	ID	V _{IL}	V _{IH}	V _F	V_R	V _{RH}	V _{max}	Vcc	V _{ccl}	V _{CCH}
o°c [19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5. 5
+25°C [19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5
+75°C	19	23	-2.0		-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5

		Pin			3002 1	est Lim	its							TEST	T CURR	ENT /	VOLTA	GE APPLIE	D TO PINS LI	STED BEL	OW:			
		Under	0	°C	+2	5°C	+7	5°C		-		1	T .	1				т	, ,					
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OLI	I _{OL2}	ОН	l _{in}	I _D	Vil	V _{IH}	V _F	V _R	V _{RH}	V _{max}	Vcc	V _{ccι}	V _{CCH}	Gnd
input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	m Adc	-	-	-	-	-	-	-	1	-	2	-	-	14	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	1	-	2		-	-	14	7*
Leakage Current	I _R	1	-	80	-	80	-	80	μ Adc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	2,7*
Breakdown Voltage	BVin	· 1	-	-	5,5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2,7*
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	7 *
Output Output Voltage	V _{OL 1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	-	1	-	-	-	-	-	14	-	2,7*
	V _{OL 2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	-	1	-	-	-	-	-	-	14	2,7*
	V _{ОН}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	1	-	-	-	-	-	-	14	-	2, 7 *
Short-Circuit Current	I _{SC}	3	-	-	-30	-100	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 3, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	38	-	-	mAde	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I _{PDH}	14	-	43	-	43	-	43	mAde	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	. *	-	7
	I _{PDL}	14	-	27	-	27	-	27	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters										Pulse In	Pulse Out							-						
Turn-On Delay	t _{pd''0''}	1, 3	-	-	-	10	-	-	ns	1	3] -	-	-	-	-	-	-	-	-	14	-	-	2, 7*
Turn-Off Delay	t pd''1''	1, 3	-	-	-	10	_	-	ns	1	3	-	-	-	-	-	-	-	-	-	14	-	-	2, 7 *

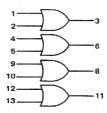
^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MTTL III MC3000 series

MC3003



This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

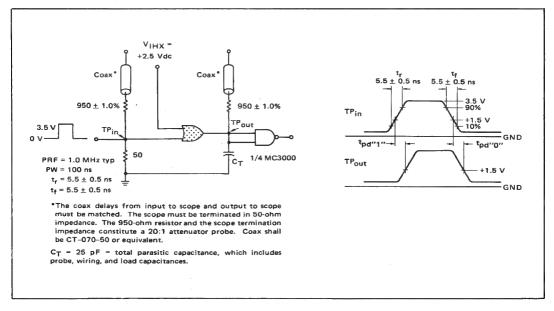


Positive Logic: 3 = 1 + 2 Negative Logic: 3 = 1 · 2

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gates are tested in the same 5—manner. Further, test procedures are shown 9—for only one input of the gate under test. 10—To complete testing, sequence through re- 12—maining inputs. 13—



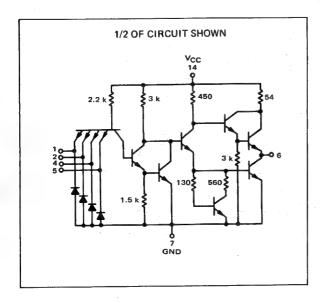
- 1							TES	T CURI	RENT/VOLT	AGE VALUES	5				
@Test		n	nA							Vo	olts				
Temperature	lori	I _{OL2}	Юн	l _{in}	Ι _D	V _{IL}	V _{IH}	V _F	V_R	V _{RH}	V _{max}	V _{cc}	V _{cci}	V _{CCH}	V _{IHX}
0°C	19	23	-2.0		-	1.1	2.0	0.4	2.5	4.0	-	5. 0	4.5	5.5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C_	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5. 5	

								7/3 C	19	23	-2.0		L	0.9	1.8	0.4	2.5	4.0		5.0	4.5	5.5	-	Į
	Pin												TEST	CURR	RENT / '	VOLTA	GE APPLIE	TO PINS LI	STED BEL	.OW:				
	Under					_]	 	T :	Τ.	Τ.	Τ.	Γ	T	T	T		F		C	T		1
Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OLT	OL2	ОН	lin	l _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{mex}	Vcc	Accr	V _{CCH}	V _{IHX}	Gnd
I _{F 1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2 *	-	-	14	-	-	7
I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	- 1	-	-	1	-	2 *	-	-	-	14	-	7
IR	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1		-	-	-	14	-	2,7
BV _{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-		-	-	-	14	-	2,7
v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-		-	-	14	-		7
v _{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1	-	-	-	2*	-	-	14	-	-	7
V _{OL2}	3	-	0.4	-	0.4	-	0, 4	Vdc	-	3	-	-	-	1	-	-	-	2*	-	-	-	14	-	7
v _{ОН}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	-	1	-	-	2*	-	-	14	-	-	7
Isc	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	1,2*	-	14	-	-	-	3,7
I _{max}	14	-	-	-	45	-	-	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-		7
IPDH	14	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	14	-	-	-	7
I _{PDL}	14	-	55	-	55	-	55	m Adc	-	-	-	-	-	, -	-	-	-	-	-	14	-	-	-	1,2,4,5,7, 9,10,12,13
									Pulse In	Pulse Out					-									
t _{pd''0''}	1, 3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-	•	-	14	-	_	2	7
tpd"1"	1,3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-		-	14	-	-	2	7
	I _{F1} I _{F2} I _R BV _{in} V _D V _{OL1} V _{OL2} V _{OH} I _{SC} I _{max} I _{PDH} I _{PDL}	Symbol Under Test IF1 1 IF2 1 IR 1 BVin 1 VD 1 VOL1 3 VOL2 3 VOH 3 ISC 3 Imax 14 IPDH 14 IPDL 14	Symbol Under Test O Min IF1 1 - IF2 1 - IR 1 - BVin 1 - VD 1 - VOL1 3 - VOL2 3 - VOH 3 2.5 ISC 3 - Imax 14 - IpDH 14 - IpDL 14 - Epd"0" 1,3 -	Symbol Prin Under Test O°C Ist Min Max IF1 1 - -1.9 IF2 1 - -2.3 IR 1 - 80 BVin 1 - - VD 1 - - VOL1 3 - 0.4 VOL2 3 - 0.4 VOH 3 2.5 - Imax 14 - - Imax 14 - 32 IpDL 14 - 55	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Pin Under Test Min Max Min Min	$ \frac{\text{Pin Under Vymbol}}{\text{Verbol}} = \frac{\text{Pin Under Voltage}}{\text{Verbol}} = \frac{\text{Verbol}}{\text{Verbol}} = \frac{\text{Verbol}}{Verbo$	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$ \frac{\text{Pin}}{\text{Symbol}} \frac{\text{Pin}}{\text{Tes}} = \frac{\text{Pin}}{\text{O'C}} - \frac{\text{Pin}}{2.5^{\circ}} - \frac{\text{Pin}}{\text{O'N}} - \frac{\text{Pin}}{\text{Pin}} - \frac$

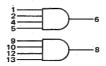
^{*}Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to $\mathbf{V}_{\mathbf{RH}}$

MTTL III MC3000 series

MC3026



This device consists of two 4-input AND power gates. Each gate is designed for driving high fan-out loads (20).

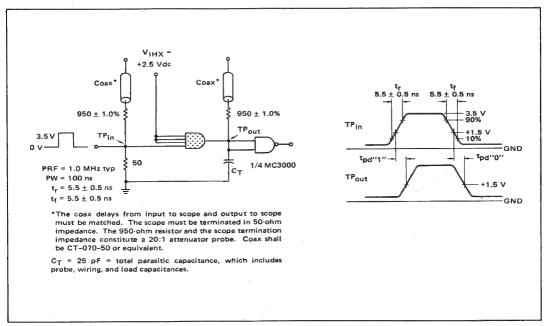


Positive Logic: 6 = 1 • 2 • 4 • 5 Negative Logic: 6 = 1 + 2 + 4 + 5

Input Loading Factor = 1.1
Output Loading Factor = 20

Total Power Dissipation = 90 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

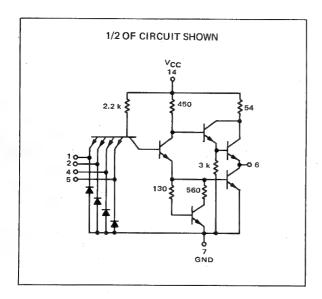


							TEST	CURR	ENT/VOLT	AGE VALUES					
@Test		n	nA							V	olts				
Temperature	l _{oti}	l _{OL2}	I _{OH}	l _{in}	I _D	V _{IL}	VIH	V _F	V_R	V _{RH}	V _{max}	V _{cc}	V _{ccl}	V _{CCH}	V _{IHX}
0°C	38	46	-4.0	-	-	1.1	2.0	0.4	2.5	4.0		5.0	4.5	5. 5	
+25°C	38	46	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5
+75°C	38	46	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	_	5.0	4, 5	5.5	-

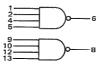
		Pin		MC	3026	Fest Lim	its							TEST	CURE	ENT /	VOLTA	GE APPLIE	TO PINS LI	STED BEL	OW:				
		Under	0	°C	+2	5°C	+7			-		Γ.	Τ.		T	T.,	T		T ,,	T	T.,	L.,	Ι	.,	1 1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OL1	OL2	ОН	'in	l _D	VIL	VIH	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	Accr	V _{CCH}	V _{IHX}	Gnd
Input Forward Current	I _{F1}	1	-	-2.1	-	-2.1	-	-2.1	mAde	-	-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	14	-	-	7
	I _{F2}	1	-	-2,6	-	-2.6	-	-2.6	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	-	14	-	7
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-		-	-	1	*	-	-	-	14	-	2, 4, 5, 7
Breakdown Voltage	BVin	1	-		5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 4, 5, 7
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	r	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	V _{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1	-	-	-	2, 4, 5 *	-	-	14	-	-	7
	V _{OL2}	6		0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	1	-	-	-	2, 4, 5 *	-	-	-	14	-	7
	V _{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6		-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	7
Short-Circuit Current	ISC	6	-	-	-50	-125	-	-	mAde	-	Ŧ	-	-	-	-	-	-	-	1, 2, 4, 5 *	-	14	-	-	-	6, 7
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	22	-	-	mAdc	-	-	-	-	-	-		-	_	1, 2, 4, 5, 9, 10, 12, 13	14	-		-	-	7
Power Supply Drain	I _{PDH}	14	-	14	-	14	-	14	mAde	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	I _{PDL}	14	-	38	-	38	-	38	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9,10,12,13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	tpd"0"	1,6	-	-	-	15	-	-	ns	1	6	-	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7
Turn-Off Delay	tpd"1"	1,6	-	-	-	15	-	-	ns	1	6	-	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7

^{*}Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to $\nu_{\rm RH}$.

MC3025



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (20).

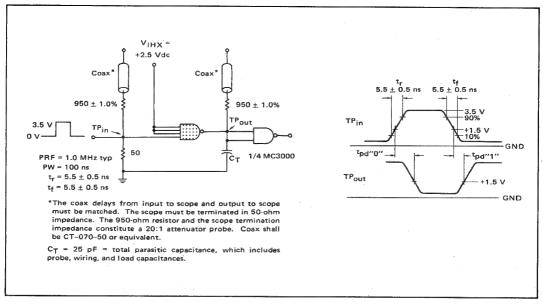


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$ Negative Logic: 6 = 1 + 2 + 4 + 5

Input Loading Factor = 1.1
Output Loading Factor = 20

Total Power Dissipation = 70 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. 12: To complete testing, sequence through remaining inputs.



1							TEST	CURR	ENT/VOLTA	GE VALUES					
@Test		n	nA							V	olts				
Temperature	I _{OL1}	I _{OL2}	I _{OH}	l _{in}	Ι _D	VIL	VIH	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	A ^{CCF}	V _{CCH}	V_{IHX}
o°c	38	46	-4, 0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5. 5	-
+25℃	38	46	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	38	46	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

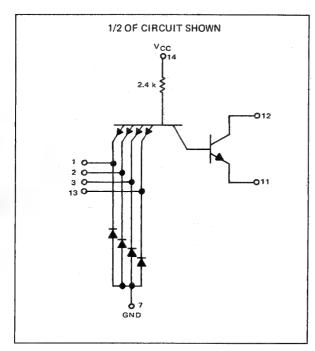
•		Pin				est Lim			,					TEST	CURE	RENT /	/OLTA	GE APPLIE	TO PINS LI	STED BEL	.0W:				
		Under	0	°C	+2	5°C		5°C				Τ.	Τ.			Tu		,,		T.,	T 14	T ,,	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	I _{OL1}	OL2	ОН	lin	l _D	VIL	VIH	V _F	V _R	V _{RH}	V _{max}	V _{cc}	Vccr	V _{CCH}	VIHX	Gnd
Input Forward Current	I _{F1}	1	-	-2.1	-	-2.1	-	-2.1	mAde	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	14	-	-	7*
	I _{F2}	1	-	-2.6	-	-2.6	-	-2.6	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	IR	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7 *
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7 *
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V _{OL1}	6	-	0.4	-	0.4	-	0.4	Vde	6	-	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V _{OL 2}	6	-	0.4		0.4	-	0.4	Vdc	-	6	-	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	7*
	V _{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6	-	-	1	-	-	-	2, 4, 5		-	. 14	-	-	7
Short-Circuit Current	Isc	6	-	-	-50	-125	-	-	mA	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	16	-	-	mAde	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7 9,10, 12, 13
Power Supply Drain	I _{PDH}	14	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	•	7
	I _{PDL}	14	-	10	-	10	-	10	mAde	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7 9, 10, 12, 13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	t _{pd''0''}	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14		_	2, 4, 5	7*
Turn-Off Delay	t pd"1".	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

^{*}Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

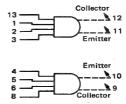
DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MTTL III MC3000 series

MC3030

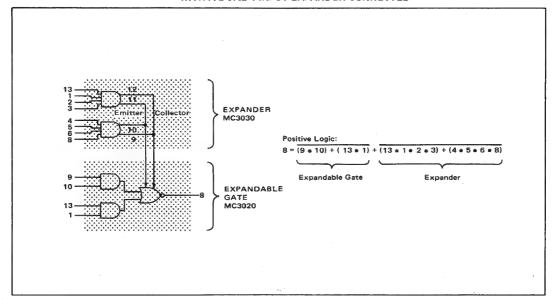


This device consists of two independent 4-input AND gates. The outputs of each gate are available as ORing nodes. Using the MC3030 expander, with the MC3020 expandable gate, up to four AND gates can be ORed together.



Input Loading Factor = 1
Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 2-WIDE 2-INPUT AND-OR-INVERT GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED



Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



				-		TEST	CURREN	IT/VO	TAGE	VALUES				
@Test			nA											
Temperature	lc	l _{in}	l _D	V _R	V _{RH}	V _F	VEET	V _{EE2}	VIH	V _{IL}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}
0°C	6.0	-	-	2.5	4.0	0.4	1.010	0.70	2.0	1. 1	-	5. 0	4.5	5. 5
+25°C	6.0	1.0	-10	2.5	4.0	0.4	0.975	0,65	1.8	1, 1	7.0	5.0	4.5	5. 5
+75°C	6, 0	-	-	2.5	4.0	0.4	0.935	0.55	1.8	0.9	-	5.0	4.5	5, 5

		Pin		MC	3030	Test Lim	nits						TES	CURE	RENT /	VOLTA	GE AP	PLIED T	O PINS	LISTED B	FLOW		0.0	1
		Under	0	°C	+2	5°C	+7	5°C		<u> </u>		_	Т		1			1				· · · · · · · · · · · · · · · · · · ·		
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	l _c	lin	l _D	V _R	V _{RH}	V _F	VEET	V _{EE2}	VIH	V _{IL}	V _{max}	Vcc	VccL	V _{CCH}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	2, 3, 13	1	-		-	-	-	-	14	-	7*
	I _{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	2, 3, 13	1	-	-	-	-	-	-	-	14	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2, 3, 7, 13
Breakdown Voltage	BVin	1	-	-	5. 5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-		-	-	14	2, 3, 7, 13*
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V _{OL}	12	-	1.41	-	1,38	-	1.34	Vdc	12	-	-	-	-	-	11	-	1	-	-	-	14	-	7*
Emitter Current	I _{EO}	11	-	-300	-	-300	-	-300	μAdc	-	-	-	-	-	-	-	11	-	1	-	-	12, 14	-	7**
Collector Current	I _{CO}	12	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	11	1	-	-	-	12, 14	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	7,0	-	-	mAdc	-		-	-		-	-	-	-	-	14	-	-	-	1,2,3,4,5, 6,7,8,13
Power Supply Drain	PDL	14	-	5.0	•	5.0	-	5, 0	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-		1,2,3,4,5, 6,7,8,13

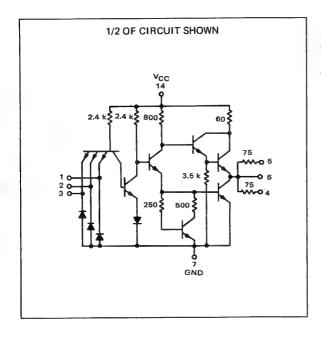
^{*} Ground inputs to gates not under test unless otherwise noted.

^{**} The inputs to both gates are ungrounded.

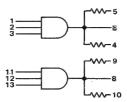
DUAL 3-INPUT 3-OUTPUT "AND" SERIES TERMINATED LINE DRIVER

MTTL III MC3000 series

MC3028



This device lin a dual 3-input/3-output series-terminated AND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6, = 1 · 2 · 3 Negative Logic: 4, 5, 6, = 1 + 2 + 3

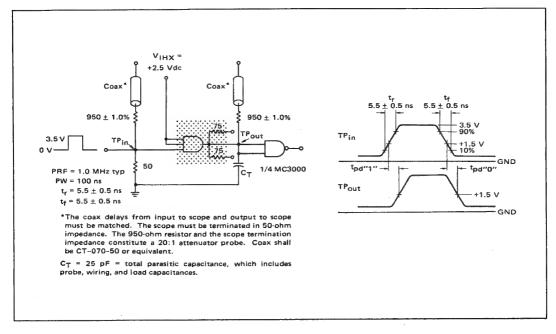
Input Loading Factor = 1

Output Loading Factor, Direct Output (Pins & & 8) = 10 minus the number of resistor-terminated outputs being used.

Output Loading Factor, Resistors (Pins 4, 5, 9, & 10) = 1

Total Power Dissipation = 56 mW typ/pkg Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver being tested. To complete testing, sequence through remaining inputs.



									TEST	CUR	RENT/\	OLTAG	E VAL	UES			-				
@Test					m	A .										Volts	:				
Temperature	l _{ol 1A}	I _{OL 18}	OLIC	I _{OL 2A}	OL 28	I _{OL 2C}	l _{oh a}	I _{OH B}	OHE	l _{in}	l _o	Va	ViH	V _F	V _R	V _{RH}	V _{mex}	V _{cc}	A ^{ccr}	V _{CCH}	V _{IHX}
0°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
+25°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	15. 2	1.9	1.9	18.4	2,3	2.3	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

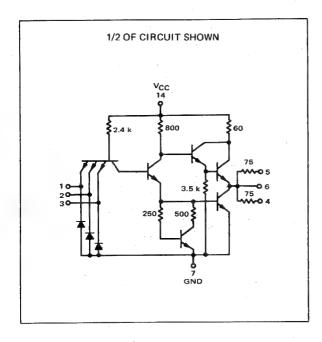
		Pin				Test Lin							•	-			TEST CUI	RRENT /	VOLT.	AGE AF	PLIED	TO PIN	IS LIST	ED BELOW	:			-			1
	l	Under	0	<u> </u>		5°C	+7.			ļ. —	Π.	ī	T ₁		Τ,	Τ.	4	1	Ti	Ti	V	v	1/	· ·	Т.,	14	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	1 11	Γ.,	, u	1
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OL 1A	OL 18	OL 10	OL 2A	OL 28	OL 2C	AHO	OHB	OHC	'in	l _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	VIHX	Gnd
input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	m.Adc	-	-	-	-	-	-	-	-	-	-	-	-		1	-	2,3*	-	-	14	-	-	7
	IF2	1	-	-2.3	-	-2.3	-	-2.3	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3*	-	-	-	14	-	7
Leakage Current	I _R	1	-	80	-	80	-	80	μAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	•	-	-	-	14	-	2, 3, 7
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	·-	-	-	-	1	-	-	-	-		•	-	-	-	14	-	2,3,7
Clamp Voltage	v _D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	V _{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	V _{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	-	-	6	5	4	-	-	-	-	-	1	-	-	-	2,3*	-	-	-	14	-	7
	V _{OL 3}	5	-	0,5	-	0,5	-	0.5	Vdc	6	5	4	-	-	-	-	-	-	-	-	1	-	-	-	2,3*	-	-	14	-	-	7
	V _{OL 4}	5	-	0.5	-	0.5	-	0.5	Vdc	-	-	-	6	5	4	-	-	-	-	-	1	-	-	-	2,3*	-	-	-	14	-	7
	v _{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	-	-	-	6	5	4	-	-	-	1	-	-	2,3 *		-	14	-	-	-7
Short-Circuit Current	Isc	6	-	-	-30	-100	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3*	-	14		-	-	6,7
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	18	-	-	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	14	-	-	-	-	7
Power Supply Drain	I _{PDH}	14	-	12	-	12	-	12	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-		1, 2, 3, 11, 12, 13	-	14	-	-	-	7
	I _{PDL}	14	-	24	-	24	-	24	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7 11, 12, 13
Switching Parameters										Pulse In	Pulse Out																				
Turn-On Delay	pd"'0"	1, 6	<u> </u>	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	·	-	~	•	-	14	-	-	2, 3	7
Turn-Off Delay	t _{pd"1"}	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2,3	7

^{*}Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to $V_{\rm RH}$.

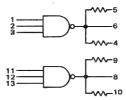
DUAL 3-INPUT 3-OUTPUT "NAND" SERIES TERMINATED LINE DRIVER

MTTL III MC3000 series

MC3029



This device is a dual 3-input/3-output series-terminated NAND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6 = $1 \cdot 2 \cdot 3$ Negative Logic: 4, 5, 6 = 1 + 2 + 3

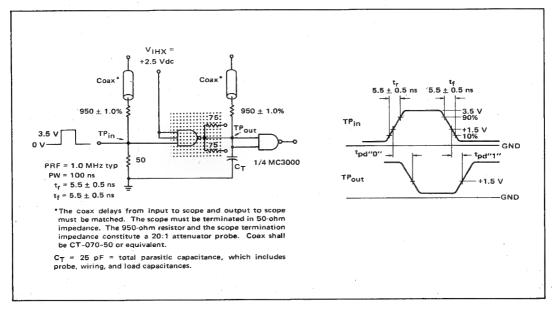
Input Loading Factor = 1

Output Loading Factor, Direct Output (Pins 6 and 8) = 10 Minus The Number of Resistor-Terminated Outputs Being Used.

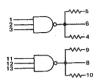
Output Loading Factor, Resistors (Pins 4, 5, 9 and 10) = 1

Total Power Dissipation = 44 mW typ/pkg Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT



Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procecures are shown for only one input of the line driver under test. To complete testing sequence through remaining inputs.



									TEST	CURR	ENT/\	OLTAG	E VAL	JES							
@Test					m	A										Volts					
Temperature	l _{OL 1A}	l _{OL 18}	l _{OL 1C}	I _{OL 2A}	I _{OL 25}	I _{OL 2C}	I _{OH A}	I _{OHB}	I _{OH C}	l _{in}	I _D	V _{IL}	VIH	V _p	V _R	V _{RH}	V _{max}	Vcc	V _{ccı}	V _{CCH}	V _{IHX}
0°C	15, 2	1.9	1, 9	18.4	2.3	2,3	-1.8	-0, 1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5. 5	-
+25°C	15. 2	1.9	1.9	18.4	2.3	2.3	-1.8	-0, 1	-0, 1	1.0	-10	1,1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5. 5	2.5
+75°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.B	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5, 5	

					WC30	029 Tes	e limie		.,,, .		1	1, 2,0	10.4	1 214	2.0	-8.0	TOT CH	-0.5	10.5	.05.40		1 4.0			4.0		1 5.0	4.5	5.5	-	1
		Pîn Under	0	°c	+2			5°C]	EST CUI	RENT /	VOLTA	AGE AF	PLIED	TO PIN	es list	ED BELOW	:						
Characteristic	Symbol	Test	Min	Max	Min		Min		Unit	I _{OL 1A}	OL 18	I _{OL 10}	I _{OL 2A}	I _{OL 28}	lot 20	I _{OH A}	I _{OH B}	I _{ОН С}	1 _{in}	I _D	V _{IL}	V _{tH}	V,	V _R	V _{RH}	V _{mex}	Vcc	V _{cc} L	V _{CCH}	V _{HOC}	Gnd
Input Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1,9	mAdc	-	-	-	-	·	-	-	-	-	-	-	-	-	1	-	2, 3		-	14		-	7*
	I _{F2}	1	-	-2.3	-	-2.3	•	-2.3	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	-	14	-	7*
Leakage Current	I _R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	-	-	٠	-	1	-	-	-	-	14	-	2, 3, 7*
Breakdown Voltage	BVin	1	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-		-	-	1	-	-	-	-	-	-	-	-	-	14	-	2,3,7*
Clamp Voltage	V _D	1	-	-	-	-1.5	*	-	Vdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	- ;	-	-	14	-	-	7*
Output Output Voltage	V _{OL 1}	6	-	0,4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	-	-	-	-	1	-	-	2, 3	-	-	14	-	-	7*
	V _{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	-	-	6	4	5	-	-	-	-	-	-	1	-	-	2, 3	-	-	-	14	-	7*
[V _{OL 3}	5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	-	-	-	-	1	-	-	2,3	-	-	14	-	-	7*
[V _{OL 4}	5		0, 5	-	0.5	-	0.5	Vdc	-	-	-	6	4	5	-	-	-	-	-	-	1	-	-	2,3	-	-	-	14	-	7*
	νон	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	-	-	-	6	4	5	-	-	1	-	-	-	2, 3	-	-	14	-	-	7*
Short-Circuit Current	ISC	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 6, 7 *
Power Requirements (Total Device) Maximum Power Supply Current	Imax	14	-	-	-	12	-	-	mAdc		-	-	-	-	-	-	-	-	-		-	-	-	-	-	14	-	-	-	-	1, 2, 3, 7, 11, 12, 13
Power Supply Drain	I _{PDH}	14	-	18	-	18	-	18	mAde	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	14	-	-		7
	1 _{PDL}	14	-	9	-	9	-	9	mAde	-	-	-	-	-	-	-	-	-	-	-		-	-	-	-	-	14	-	-	-	1, 2, 3, 7, 11, 12, 13
Switching Parameters Turn-On Delay	t _{pd"0"}	1,6	_	_	_	10	_		ūs.	Pulse in	Pulse Out	_	_	_			_		_	_	_	_	_			-	14	-	_	2, 3	7*
Turn-Off Delay	t _{pd"1"}	1,6	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14		-	2,3	7*

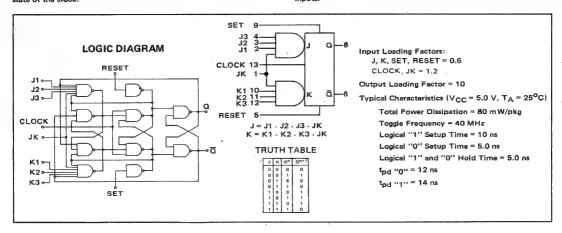
^{*}Since this ■ an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

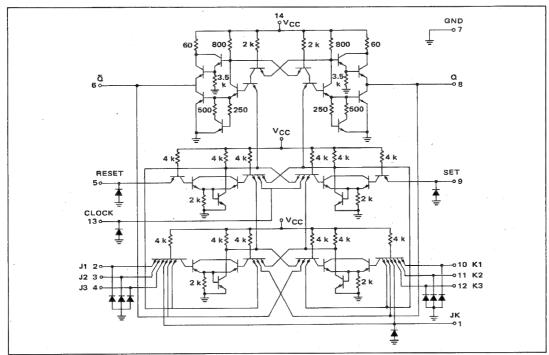
"AND" J-K FLIP-FLOP

MC3050

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set-up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Ω and $\bar{\Omega}$ respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs





OPERATING CHARACTERISTICS

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

Unused Inputs:

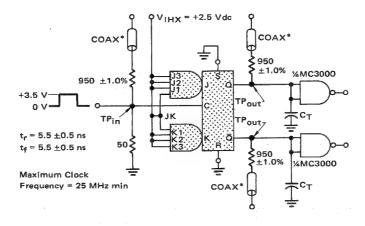
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, \overline{Q} , or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

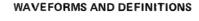
Unused SET and RESET inputs MUST be tied to ground.

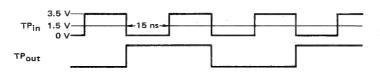
FIGURE 1 - MAXIMUM CLOCK FREQUENCY TEST CIRCUIT

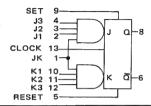


*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.







						TEST C	URREN	T/VO	LTAG	VALUES				
@ Test		n	ıΑ							Volts				
Temperature	lor	I _{ОН}	l _{in}	21 _{in}	I _D	VIL	V _{IH}	V _F	\forall_{R}	V _{RH}	V _{max}	V_{CC}	VCCL	V_{CCH}
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

		Pin			-	Test L	_				-		TEST	CUR	RENT/	/OLTA	GE AP	PLIED	TO PINS LISTED BI	ELOW:				
Characteristic	Symbol	Under Test		°C May		5°C Max		/5°C Max	Unit	lor	loh	l _{in}	2l _{in}	I _D	VIL	VIH	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}	Gnd
	Зуньон	1631	MILLE	Max	141111	IVIAX	141111	Max	Ullit	- OL	On	-"	- 111	۳	- "	107			NII .	11107		-	CCIA	
Input Forward Current	I _{FJ}	2 3 4	-	-1.5	-	-1.5	-	-1.5	mAdc		-	- - -	-	-	-	-	2 3 4	1 1	1,3,4,5 1,2,4,5 1,2,3,5	- ·		-	14 	7,9,13
	IFK	10 11 12	- 1	-1.5	-	-1.5	- - -	-1.5	mAdc		-	-	-	- 1	-	1	10 11 12	1 1	1,9,11,12 1,9,10,12 1,9,10,11	- - -	-	- - -	14	5,7,13
	I _{FC}	13	-	-3.0	-	-3.0	-	-3.0	m Adc	-		-	-		7 -	-	13	-	4 - j	- ,	-	-	14	1,5,7,9
	IFJK	-1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	2,3,4,10,11,12	-	1,	-	14	5,7,9,13
	IFS	9	-	-1.5	-	-1.5	-	-1.5	m Adc	-	-	-	-	-	-		9	-	5	-			14	. 7
	· I _{FR}	5 .		-1.5	-	-1.5	-	-1.5	m Adc	-	-	-	-	-	-	-	5	-	9	-	-	-	14	7
Leakage Current	I _{RJ}	2 3 4		80	-	80	-	80	μAdc ↓	-	-	-	- 1		-	-	-	2 3 4	9	- 1	-	-	14	1,3,4,5,7 1,2,4,5,7 1,2,3,5,7
	IRK	10 11 12	-	80	-	80		80	μAdc		- - -	-	- - -	- - -		-	-	10 11 12	5			-	14	1,7,9,11,12 1,7,9,10,12 1,7,9,10,11
	IRC	13	-	110	-	110	-	110	μAde	-	-	-	-	-	-	-	-	13	1,2,3,4,5,10,11,12	-	-	-	14	7,9
	I _{RJK}	1	-	110	-	110	-	110	μAde	-	-	-	-	-	-	-	-	1	9	-	-	-	14	2,3,4,5,7,10,11,12
	IRS	9	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	9		-	7-	-	14	7
	I_{RR}	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	14	7

ELECTRICAL CHARACTERISTICS (continued)

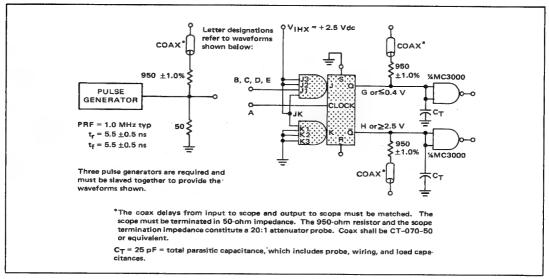
<u> </u>						TEST C	URREN	IT/VO	LTAG	E VALUES				
@ Test		n	ıΑ							Volts				
Temperature	lor	I _{ОН}	Iin	21 _{in}	l _D	V _{IL}	VIH	V _F	$V_{\mathbf{R}}$	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V_{CCH}
0°C	23	-2.0	T -	-	-	1.1	2.0	0.4	2.5	4. 0		5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	10	1.1	1.8	0.4	2. 5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4. 0	-	5.0	4.5	5.5

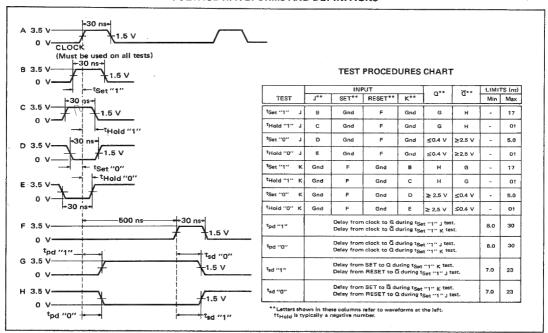
				3400	2050	Total 1	inside		1,50															
		Pin				Test L							TEST	CUR	RENT/\	/OLTA(SE API	PLIED	TO PINS LISTED BI	ELOW:				
Characteristic	Symbol	Under Test	Min	Max	_	5°C Max		5°C Max	Unit	l _{OL}	ОН	l _{in}	2l _{in}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{ссн}	Gnd
Breakdown Voltage	BV	2 3	-	-	5.5	-	-	-	Vdc 	-	-	2	-	-	-	=	-	-	9 	-	-	-	14	1,3,4,5,7 1,2,4,5,7
		4 10		-		-	-	-		-	-	10	-	-	-	-	-	-	5	-		-		1,2,3,5,7 1,7,9,11,12 1,7,9,10,12
		11 12 13	-	Ξ.		-	- -	-		-	-	11 12	13	-	-	-	-	-	1,2,3,4,5,10,11,12	-		-		1,7,9,10,12 1,7,9,10,11 7,9
		1 9	-	-		-	-	-		=	-	9	1 -	-	-	-	-	-	9	-	-	-		2,3,4,5,7,10,11,12
		5	-	-	*	-	-	-	1	-	-	5	-	-	-	-	-	-	-	-		-	*	7
Clamp Voltage	V _D	2 3 4	-	-	-	-1.5	-	-	Vdc	-	-	-	-	3 4	-		-	-	-	-	-	14	- -	7
		10 11	-	-	-		-	-		-	-	-	-	10 11	-	-	-	-		-	-		-	
		12 13	-	-	-		-	- '		7	-	-	-	12 13	-	-	-	-	-	-	-		-	
·		9 5	-	-	-		-	-		-	-	-	-	9 5	-	-	-	-	-	-	- - -		-	•
Output Output Voltage	V _{OL}	6 8	-	0.4	-	0.4	-	0.4	Vdc Vdc	6 8	-	-	-	Ξ	5 9	9 5	-	-	-	-	-	-	14 14	7,13 7,13
	v _{OH}	6 8	2.5	-	2.5 2.5	-	2.5 2.5	-	Vdc Vdc	-	6 8		-	-	9 5	5 9	-	- -	- \	-	-	14 14	-	7,13 7,13
Short-Circuit Current	I _{SC}	6 8	-	-	-30 -30	-100 -100	-	-	mAde mAde	=	=	-	-	-	-	-	-	-	5 9	_	14 14	-	Ξ	6,7,9 5,7,8
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	35	_	-	mAdc	-	-	-	-	-		-	-	-	-	14	-	-	-	1,5,7,13
Power Supply Drain	I _{PD}	14	-	26	-	26	-	26	mAdc	-	-	-	- "	-	-	-	-	-	-	-	14	-	-	1,5,7,13

OPERATING CHARACTERISTICS (continued)

FIGURE 2 - SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)

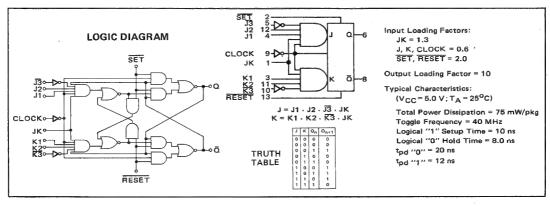


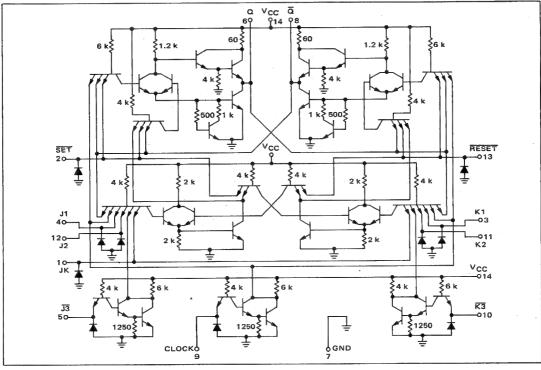


MC3052

The MC3052 is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a J-input ANDed together and two K-inputs and a K-input ANDed together. An enable input (JK) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, J, K and K) or an additional logic input (JK) for use in counters or certain other applications. A direct SET and RESET are provided to enable presetting data into the flip-flop such as initial conditions. The direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state, since the inputs are inhibited under this condition. Information may be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct SET or RESET provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct SET or RESET inputs.





ELECTRICAL	SE'					٦																			
CHARACTERISTI	cs 3	5 - Do	\equiv).					_		,			1	EST C	URRE	NT/V	OLTAG	E VALUES						
	CL OC	к 9	止					T _i	@ est		n	ıA							Volts						
		K 1							erature	OL	ОН	l _{in} ·	21 _{in}	I _D	VIL	V _{IH}	٧	V _R	V _{RH}	V _{max}	V _{cc}	VCCL	V _{CCH}		:
	K	1 3 2 11 3 19 Do	=	}	, ;	88			0°C	23	-2.0	-	-	<u> </u>	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5]	
	RESE			_/L	_	-1			+25℃	23	-2.0	1.0	2,0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5].	
		. 1 210	, .						+75℃	23	-2.0	_		<u> </u>	0,9	1,8	0,4	2, 5	4,0	-	5.0	4.5	5.5		
		Pin	_		-	Test Li						TES	T CUR	RENT	VOLT	AGE A	PPLI	ED TO I	PINS LISTED BEL	OW:					
Characteristic	Symbol	Under Test		O°C Max		5°C Max		5°C Max	Unit	lor	Гон	l _{in}	2l _{in}	I _D	V _{IL}	VIH	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	VCCL	V _{CCH}	P,*	Gnd
Input	7					******		_	J		5			Ť			H	-		IIII			CON	ŀ	
Forward Current	I _{FJ}	4 12	-	-1.5 -1.5	-	-1.5 -1.5	-	-1.5 -1.5	mAdc mAdc	-	-	-	-	-	-	-	4 12	-	1,12 1,4	-	-	-	14 14	-	5,7,9,13 5,7,9,13
	I _{FK}	3 11	-	-1.5 -1.5	-	-1.5 -1.5	-	-1.5 -1.5	mAdc mAdc	-		-	-	-			3 11	-	1,11 1,3	- -	-	-	14 14	-	2,7,9,10 2,7,9,10
	I _F j	5	-	-1.5	-	-1.5	-	-1.5	mAdc	-		-	-	-	- 2	-	5	-	- :	-	-	-	14	-	. 7
	I _{FK}	10	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-1	-	10	-	-	-	-	-	14	-	7
	I _{FC}	9	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	, -	-	9	-	-	-	-	-	14	-	7
	I _{FJK}	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	3,4,11,12	-	-	-	14	-	2,5,7,9,10,13
	I _{FŠ}	2	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-		2	-	-	-	-	- 1	14	-	7,9,13
	$_{\mathrm{F}\overline{\mathrm{R}}}^{\mathrm{I}}$	13	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	-	13	-		-	-	-	14	-	2,7,9
Leakage Current	I _{RJ}	4 12	-	80 80	-	80 80		80 80	μAdc μAdc	-	-	-	-	-	-	-	-	4 12	5,9 5,9	-	-	1-	14 14	-	1,2,7,12 1,2,4,7
	I _{RK}	3 11	-	80 80	-	80 80		80 80	μAdc μAdc	-	-	-	-	-	-	-	-	3 11	9,10 9,10	-	-	-	14 14	-	1,7,11,13 1,3,7,13
	$I_{R\overline{J}}$	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	5	-	-	-		14	-	7
	IRK	10	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	- 1	10	-	-	-	-	14	-	7
	IRC	9	-	80	-	80	-	80	μAdc	- ,	-	-	-	-	-	-	-	9	-	-	-	-	14	-	7
	I _{RJK}	1	-	110	-	110	-	110	μAde	-	-	-	-	-	-	-	-	1	5,9,10	-	-	-	14	-	3,4,6,7,8,11,12
	$I_{R\overline{S}}$	2	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	2	1,4,10,12,13	-	-	-	14	9	3,5,7,11
	$I_{R\overline{R}}$	13	-	140	-	140	-	140	μAde	-	-	-	-	-	-	-	-	13	1,2,3,5,11	-	- J	-	14	9	4,7,10,12

*Pulse is used to set flip-flop in desired state. P1 = $\frac{4.0 \text{ V}}{0 \text{ V}}$ (V_{RH})

ELECTRICAL	
CHARACTERISTICS	(continued)

[1 1			T	EST C	URREN	IT/V	DLTAGE	VALUES				
@ Test		n	ıΑ							Volts				
Temperature	OŁ	ОН	in	2l _{in}	I _D	VIL	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	Accr	V _{CCH}
o°c	23	-2.0	-		-	1, 1	2.0	0.4	2.5	4.0	-	. 50	4.5	5.5
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0, 9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

		Pin	T	MC	3052	Test L	imits		,,,,,	20		TES	T CHP	FNT	VOLT	AGE A	PPI II	ED TO I	PINS LISTED BEL	ow.					
		Under		O°C	+2	:5°C	+7	′5°C				1 53							ING FIGURE DEF			,	-	- 1	
Characteristic	Symbol		Min	Max	Min	Max	Min	Max	Unit	lor	I _{OH}	l _{in}	2l _{in}	l _D	VIL	V _{IH} .	٧ _F	V _R	V _{RH}	V _{max}	V _{cc}	VCCL	V _{ссн}	P ₁ *	Gnd
Breakdown Voltage	BVin	4	-	-	5.5	-	-	-	Vdc	-	-	4	-	-	-	-	-	-	5,9	-	-	-	14	-	1,2,7,12
		12 3	-	-		-	-	-		-	-	12	-	-	-	-	-	_	5,9 9,10	-	-	-		-	1,2,4,7 1,7,11,13
		3 11	_	-		-	-	_		-	_	3 11	-	_	_	-	-	-	9,10	_	_	-		_	1,3,7,13
		1	_	_		-	-	_		-	_	-	1	_	-	-	-	-	2,5,9,10,13	-	_	-		-	3,4,6,7,8,11,12
		2	-			-	- 1	-		-	-	-	2	-	-	-	-	-	1,4,10,12,13	-	-	-		9	3,5,7,11
		13			.	-	-	-		-	-	-	13	-	-	-	-	-	1,2,3,5,11	-		-	1	9	4,7,10,12
- P		5 9	-	-		-	-	-		-	~	5	-		-	-	-	-	-	· -	-	-		-	7
·		10	-	_	↓	-	-	_		-	Ī.	9 10	-	-		_	-	_	_	_	-	1 [₩	-	, ,
			-		<u>'</u>	-1.5	 	-	Vdc		<u> </u>		-	4	<u> </u>		+	-			_	14	 `	+-	7
Clamp Voltage	$v_{\rm D}$	4 12	[:	_	-	-1.5	-	_	Vac	-		_	_	12		-	-	-	_	_	-	1 1 1			i
		3	-		-		1 -	_		_	_	_	-	3	-	_	-	-	-	-	-		-	-	
		11	-	-	-		-	-		-	-	-	-	11	-	-	-	-		-	-		-	-	
		5	-	-	-		-	-		-		-	-	5	-	-	-	-	-	-	-			-	
4		10 9	-	-	-		-	-		_	1 :	-	-	10	_	-	1.	-	Ī	_	-		_	_	
		ĭ] -	_ I	-		-	-		-	-	-	2.	1	-	-	-	-	-	-			-	-	
		2 13	-		-	1		-		-	-	-	_	13	-	-	_	_	<u> </u>	-	-	+	_	-	•
Output																									
Output Voltage	VOL	6 8	-	0. 4 0. 4	-	0.4	-	0.4 0.4	Vdc Vdc	6 8	-	-	-	-	13 2	2 13		-	-		-	-	14 14	_	7,9 7,9
	VOH	6 8	2. 5 2. 5	- 1. - 1.	2.5 2.5	-	2.5 2.5	-	Vdc Vdc	-	6 8	-	-	-	2 13	13 2	-	-		-	-0	14 14	-	-	7,9 7,9
Short-Circuit Current	I _{SC}	6 8	-	-	-30 -30		-	-	mAde mAde	-	-	-	-	-	-	=	-	-	-	-	14 14	-	-	-	2,6,7 7,8,13
Power Requirements																		ļ .							
(Total Device) Maximum Power Current	I _{max}	14	-	-	-	42	-	-	mAde	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7,9,10,11,12,13
Power Supply Drain	I_{PD}	14	-	30	-	30	-	-	mAdc	-	-	-	-	-	-	-	Ŀ	-	-	-	14		-	-	1,2,5,7,9,10

^{*}Pulse is used to set flip-flop in desired state. P₁ = $\frac{4.0 \text{ V (V}_{RH})}{0 \text{ V}}$

OPERATING CHARACTERISTICS

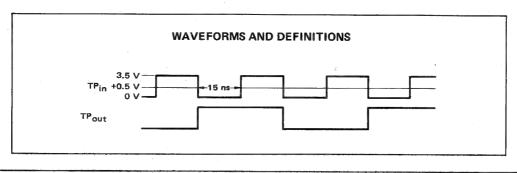
Data should be present prior to the negative clock transition. If data is changed from a "1" to a "0" while the clock is in the low state, the flip-flop will not recognize this new data state.

The application of a low level to the \widetilde{SET} input sets Q high and low level on the \widetilde{RESET} input resets Q low. These functions may be performed at any time without regard to the clock area.

Positive edge triggering — When the clock goes from the low to the high state, the information stored in the master flip-flop section is transferred to the slave flip-flop section thus appearing at the outputs. When the clock is in the high state, the inputs are inhibited.

Unused J, K, and JK inputs should be tied together with used inputs, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc. The unused \overline{J} and \overline{K} inputs must be tied to ground. The unused \overline{SET} and \overline{RESET} inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

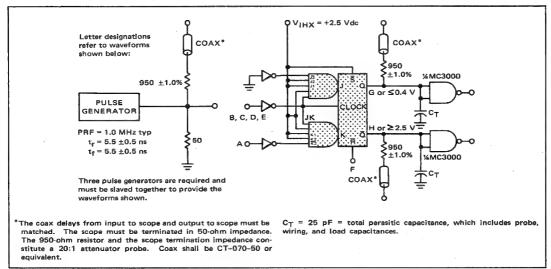
FIGURE 1 - MAXIMUM CLOCK FREQUENCY TEST CIRCUIT V_{1HX} = +2.5 Vdc COAX* COAX 950 ±1.0% **%MC3000** 950 ±1.0% +3.5 V $\mathcal{L}_{\mathsf{TP}_{\mathsf{out}}}$ TPin' 0 V TP_{out} 50 t_r = 5.5 ±0.5 ns 950 $t_f = 5.5 \pm 0.5 \text{ ns}$ +1.0% 14MC3000 Maximum Clock Frequency = 25 MHz *The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent. C_{Υ} = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

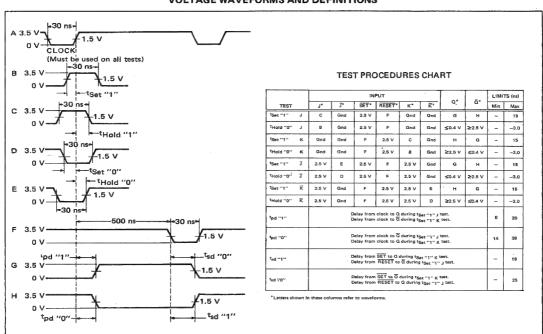


OPERATING CHARACTERISTICS (continued)

FIGURE 2 - SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)

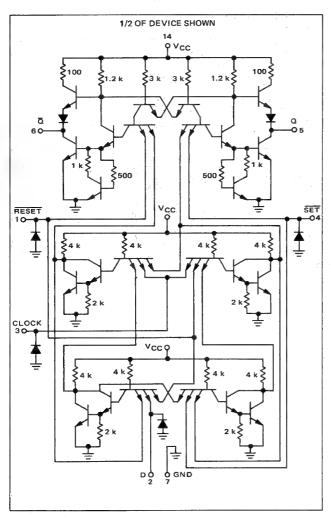




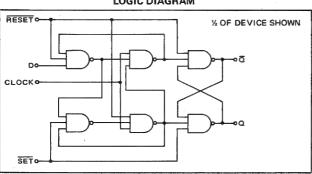
MTTL III MC3000 series

DUAL TYPE D FLIP-FLOP

MC3060



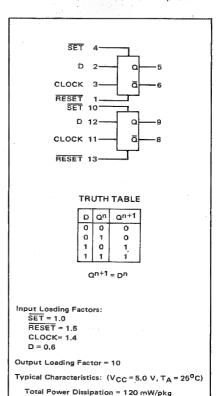
LOGIC DIAGRAM



The MC3060 dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Set-up and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Ω and $\overline{\Omega}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct SET or RESET inputs.



Toggle Frequency = 30 MHz Logical "1" Setup Time = 10 ns Logical "0". Setup Time = 5.0 ns Logical "1" and "0" Hold Times = 5.0 ns

t_{pd} "0" = 17 ns t_{pd} "1" = 15 ns

ip-flop. The other	flip-flop	is test	ed in	CLC	ск	3-	₫-6	i	1					TI	ST CH	DENT	/VOLT	ACE 1	ALUES						
same manner.				RES	ET	1	┰,		@		m	A			131 CUI	CREIN I	/ VULT	AGE V	Volts						
					ET	10-	_		Test	l _{OL}	I _{OH}		2l _{in}	I_	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	V _{CCL}	V _{CCH}		
					D	12	Q-9	Tem	perature O°C	23	-2.0	lin	- in	¹D	1.1	2.0	0.4	2.5	4, 0	max	5.0	4.5	5. 5		
				CLC	СК	11-	Q-8	1	+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5		
				RES	SET	13-			+75°C	23	-2.0	-		-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5		
		Pin			_	Test Li	mits					TEC	TCHP	ENT	/VOLTA	GE AD	DITED		NS LISTED E	EI OW.					
		Under	0	°C	+2	25°C	+7	5°C	1																
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	lor	Іон	in	2l _{in}	I _D	VIL	VIH	٧ _F	$V_{\mathbf{R}}$	V _{RH}	V _{max}	V _{cc}	Accr	V _{CCH}	P ₁ *	Gnd
orward Current	I _{FC}	3	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	3	-	1	-	-	-	14	-	2,4,7,1
	I_{FD}	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-,	-	2	- 1	1,4	-	-	-	14	-	3,7,11
	IFS	4	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	4	-	1	-	-	-	14	-	2,3,7,1
	I _{FR}	1	-	-3.4	-	-3.4	-	-3.4	mAde	1- 1	-	-	-	-		-	1	-	2,4	-	-	-	14	-	3,7,1
Leakage Current	I _{RC}	3	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	3	4	-	-	-	14	-	1,2,7,1
	I _{RD}	2	-	80	-	80	-	80	μAde	-	-	-	-	-	-	-	-	2	3,4	-	-	-	14	-	1,7,11
	I _{RS}	4	-	110	-	110		110	μAdc	-	-	-	-	-	-	-	-	4	1,2	-	-	-	14	3	7,11
	IRR	1	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	1	4		-	-	14	3	2,7,11
Breakdown Voltage	BV _{in}	3 2 4 1	- - -	- - -	5.5		-	-	Vdc		-	2 -	3 - 4 1	-	- - -	-	- - -	- - -	4 3,4 1,2 4	-		-	14	- - 3 3	1,2,7,1 1,7,11 7,11 2,7,11
Clamp Voltage	v _D	3 2	-	-	-	-1.5	-	-	Vdc I	- '	-	-	-	3 2	-	-	-	-	. [-	-	14	-	-	7,11
		4 1	-		-	+	-	-	+	-	-	-	-	1	-	-	-	-	-	-	-	1	-	-	↓
U tput Output Voltage	v _{OL}	6 5	-	0.4		0. 4 0. 4	-	0. 4 0. 4	Vdc Vdc	6 5	-	-	-	-	.4	1 4	-	-	-	-	-	-	14 14	-	2,3,7,1 2,3,7,1
	V _{ОН}	6 5	2.5 2.5	-	2. 5 2. 5	-	2. 5 2. 5	-	Vdc Vdc	-	6 5	-	-	-	1 4	4	-	-	-	-	-	14 14	-	-	2,3,7,1 2,3,7,1
Short-Circuit Current	I _{SC}	6 5	-	-	-20 -20	-60 -60	-	-	mAde mAde	-	-	-	-	-	-	4	1 4	-	-	-	14 14	-	-	- 1	6,7,11 5,7,11
				-												_	_								0,7,11
Ower Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	42	-	-	mAdc	-	-	-	~	-	-	-	-	-	1,13	14	-	-	-	-	3,4,7,10

^{*}Pulse is used to set flip-flop in desired state. $P_1 = \int_{0}^{4.0} V(V_{RH})$. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

OPERATING CHARACTERISTICS

Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

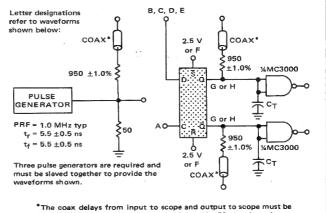
The direct SET and RESET inputs may be used at any time as they completely override the clock.

Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.



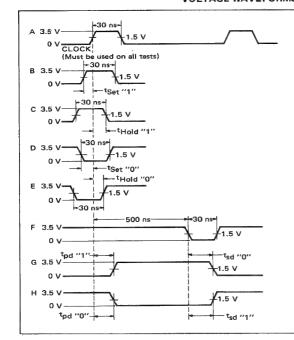
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

 $C_{\mbox{\scriptsize T}}=25~\mbox{\scriptsize pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

			INPL	JT		.	LIMI	TS (ns)
TEST		D*	SET*	RESET*	a*	₫°	Min	Max
^t Set "1"	D	В	2.5 V	F	G	н	-	15
^t Hold "1"	D	С	2.5 V	F	G	н	-	6.0
t _{Set} "0"	D	D	F	2.5 V	н	G	-	15
tHold "O"	D	E	F	2.5 V	н	G	-	5.0
[†] pd "1"			Set "1"	n clock to Č			10	25
^t pd ''0''		t	Set ''0''	n clock to Ĉ		-	10	25
¹ sd "1"		,	Set ''0''	n RESET to			5.0	20
^t sd "0"		1	Set "0"	n RESET to				20

^{*}Letters shown in these columns refer to waveforms at left.

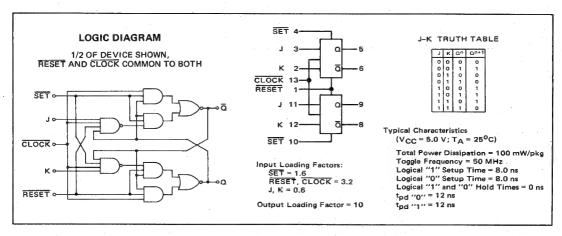
DUAL J-K FLIP-FLOP

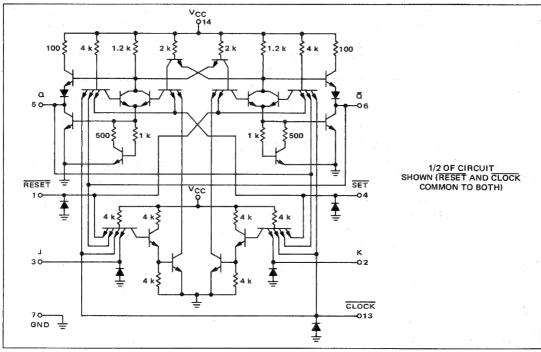
MC3061

The MC3061 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input in addition to the common direct RESET input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Setup and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input. In addition, both flip-flops may be reset simultaneously by using the common RESET in a similar manner.





Test procedures are shown for only one flip-flop plus the inputs common to both flip-flops. To complete testing, sequence through the remaining inputs in the same manner.



					TES	ST CUP	RENT	VOLT	AGE V	ALUES				
@ Test		m	Α							Volts				
Temperature	loL	l _{он}	l _{in}	21 _{in}	۵٦	V _{IL}	VIH	٧ _F	V _R	V_{RH}	V _{max}	V _{cc}	V_{CCF}	V_{CCH}
0°C	23	-2.0	-	- '	-	1.1	2.0	0.4	2. 5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5, 0	4.5	5.5
+75°C	23	-2.0	-	-		0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

		Pin		MC	3061	Test L	imits					TES	T CUR	RENT	/VOLT	AGE A	PPLIED	TO F	INS LISTED I	BELOW:					
		Under		°C		5°C		5°C		 								,		v	_	14	W	D *	٠١
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OF	НО	in	2l _{in}	¹D	V _{IL}	V _{IH}	V _F	V _R	V _{RH}	V _{max}	V _{cc}	VCCL	V _{CCH}	P ₁ *	Gnd
Input Forward Current	I_{FJ}	3	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	3	-	1,4,13	-	-	-	14	1	2,7,10
	IFK	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	2	-	1,4,13	-	-	-	14	4	3,7,10
-	I _{FR}	1	-	-3.5	-	-3.5	-	-3.5	mAdc	-	-	-	-	-	-	-	1	-	3,4,13	-	-	-	14	-	2,7,10
	I _{FS}	4	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-		-	4		1,2,13	-	- 1	-	14	-	3,7,10
	I _F C	13	-	-5.7	-	-5.7	-	-5.7	mAdc	-	-	^	-	-	-	-	13	-	1,2,3,11,12	-			14	4,10	7
Leakage Current	I _{RJ}	3	-	80	-	80	-	80	μAdc	-	-	-	-1	-	-	-	-	3	2,4	-			14	-	1,7,10,13
	IRK	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	2	1,3	-	-	-	14	-	4,7,10,13
	I _{RR}	1	-	230	-	230	-	230	μAdc	-	-	-	-	-	-	-	-	1	2	-	-	-	14	1	3,4,7,11,13
	IRS	4	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	4	. 3	-	-	-	14	4	1,2,7,10,13
	I _{RC}	13	-	290	-	290	-	290	μAde	-		-	-	-	-	-	-	13	-	-	- 1	-	14	-	1,2,3,4,7,10,11,12
Breakdown Voltage	BV _{in}	3 2 1 4 13	-	-	5.5	-	-		Vdc	-	-	3 2 -	- 1 4 13	-		-		-	2,4 1,3 2 3	- :	-	-	14	- 1 4	1,7,10,13 4,7,10,13 3,4,7,11,13 1,2,7,10,13 1,2,3,4,7,10,11,12
Clamp Voltage	v _D	3 2 1 4 13	-	-	- - - -	-1.5	-	-	Vdc		-	-	-	3 2 1 4 13	-		-		- - - -	-	-	14		-	7,10
Output Output Voltage	V _{OL}	5	-	0.4	-	0.4 0.4	-	0.4 0.4	Vdc Vdc	5 6		-	-	1 1	1 4	4	-		-	-		- -	14 14	1 4	7,10 7,10
	VOH	5 6	2.5 2.5	-	2.5 2.5	-	2.5 2.5	1.	Vdc Vdc	-	5 6	-	-	-	4	1 4	-	-	-	- ,	-	14 14	-	4	7,10 7,10
Short-Circuit Current	I _{SC}	5 6	=	-	-20 -20	-60 -60		-	mAdc mAdc	-	-	-	-	1 1	-	-	-	-	-	-	14 14	-	-	-	4,5,7,10 1,6,7,10
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14		-	-	42		-	mAde	-	-	-	-		-	-	-		- "	14	-	-	•	-	4,7,10
Power Supply Drain	IPD	14	-	30		30	-	30	mAde	-	-	-	-	-	-	-	-	-	- :	-	14	-	-	-	1,7

^{*}Momentarily ground pin prior to taking measurement. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

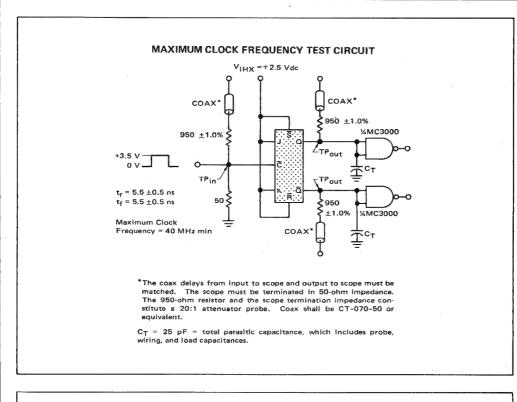
High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

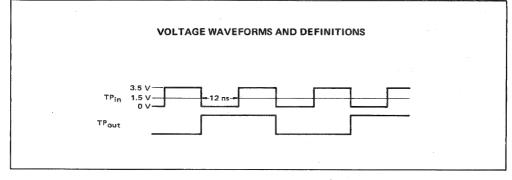
The direct $\overline{\text{SET}}$ (individual) inputs and $\overline{\text{RESET}}$ (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{\text{SET}}$ input or reset to the Q = 0 state by applying a low level to the $\overline{\text{RESET}}$ input. If these inputs are not used they should be returned to a volt-

age between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

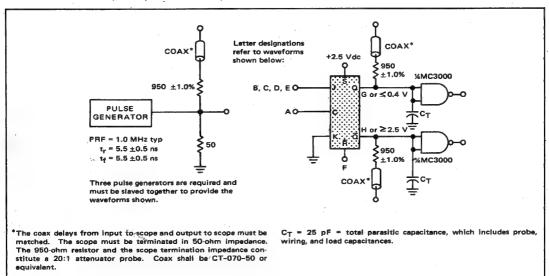


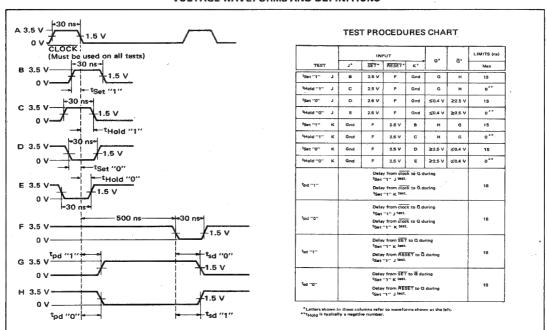


OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs and RESET Input; to test other inputs, refer to Test Procedures Chart)





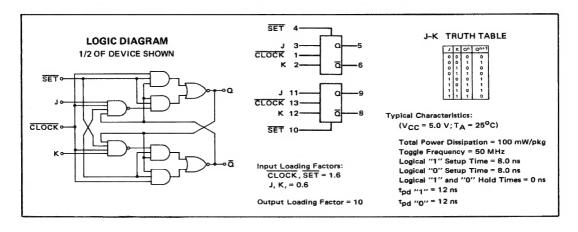
DUAL J-K FLIP-FLOP

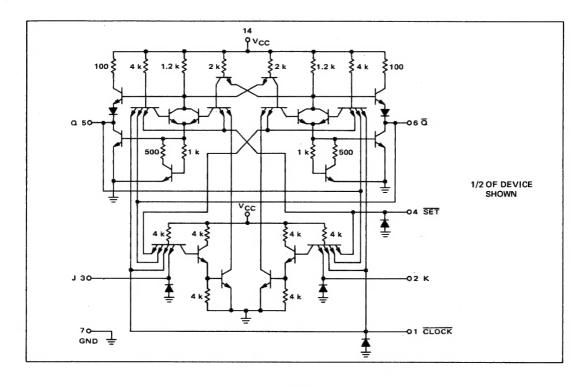
MC3062

The MC3062 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

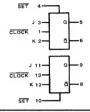
Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Set-up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the SET input.





Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



_				TES	T CUF	RENT	VOLT	AGE VA	LUES			
@ Test		r	nA					Vo	olts			
Temperature	lor	loH	l _{in}	2I _{in}	, I _D	V _F	VR	V _{RH}	V _{max}	V _{cc}	VCCL	V _{CCH}
0°C	23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	-10	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5

		Pin		MC3	062	Test Li	imits				TI	ST CII	RRENT	/VOI	TAGE	APPI IF	D TO PI	NS LISTEI	RELOV	٧.			
		Under)°C	+2	:5°C	+7	5°C									r				I.,		
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	OL	, IOH	lin	2I _{in}	l _D	V _F	V _R	V _{RH}	V _{max}	V _{cc}	VCCL	V _{CCH}	P ₁ *	Gnd
nput Forward Current	$\mathbf{I_F}$	2 3	1 1	-1.5 -1.5	<u>-</u>	-1.5 -1.5	-	-1.5 -1.5	mAdc mAdc	-	-	-	. 1 1	1 1	2 3	-	1,4 1,4		-	-	14 14	-	3,6,7,13 2,5,7,13
	I _{FS}	4	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-	4	, -	1,2	-	-	-	14	-	3,7,13
	I _F C	1	-	-2.9 -2.9	-	-2.9 -2.9	-	-2.9 -2.9	m Adc m Adc	-	-	-	-	-	1 1	-	2,3 2,3,4	-		-	14 14	4 5	7,13 7,13
Leakage Current	IR	2 3	-	80 80	-	80 80	-	80 80	μAdc μAdc	-	-	-	-	- 1	-	2	3 2	-	-	-	14 14	-	1,4,7,13 1,4,7,13
	$I_{R\overline{S}}$	4	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	4	3	-	-	-	14	-	1,2,7,13
×	I _R C	1		170	-	170	-	170	μAdc	-	-	-	-	- ,	-	1	- 1	-		-	14	-	2,3,4,7,13
Breakdown Voltage	BV _{in}	2 3 4 1	-	-	5.5	-			Vdc	- - -		2 3 - -	- - 4 1	-	-	-	-	-			14		1,4,7,13 1,4,7,13 1,2,7,13 2,3,4,7,13
Clamp Voltage	v _D	2 3 4 1		-		-1.5		1 1 1	Vdc	-		-		2 3 4 1	- - -	-	-			14	-	1111	7,13
Output Output Voltage	v _{ol}	5 6	-	0, 4 0, 4	-	0.4 0.4	-	0.4	Vdc Vdc	5 6	-		-	-	4	-	-	-	-	-	14 14	5 4	1,7,13 1,7,13
	VOH	5 6	2.5 2.5	- v.	2.5 2.5	-	2.5 2.5	-	Vdc Vdc	-	5 6	-	-	-	4	-	4	-	-	14 14	-	4 5	7 1,7,13
Short-Circuit Current	I _{SC}	5	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	4,5,7,13
Power Requirements (Total Device) Maximum Power Supply Current	I _{max}	14	-	-	-	41		-	mAdc	-	-	-	-	-	-	-		14	-	-	-	-	4,7,10
Power Supply Drain	I _{PD}	14	-	29	-	29	-	29	mAdc	-	-	-	-	-	-	-	-	- ;	14	-	-	-	4,7,10

^{*} Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

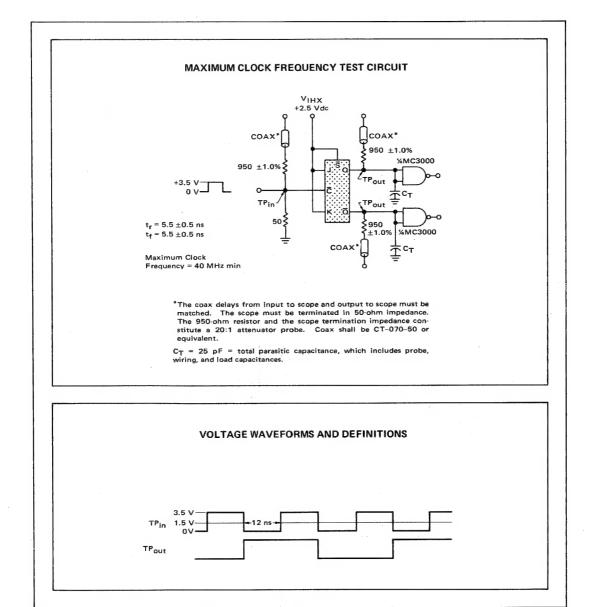
OPERATING CHARACTERISTICS

The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Q=1 state by applying a low level to the \overline{SET} input. The direct \overline{SET} inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs; to test other inputs, refer to Test Procedures Chart)

